

DELIVERY SPECIFICATION

SPEC. No. C-LMEGA-C-g

D A T E : Apr., 2022

To

Non-Controlled Copy

CUSTOMER'S PRODUCT NAME

TDK PRODUCT NAME

Multilayer Ceramic Chip Capacitors
 (Mega cap CA series)
 Tape packaging 【RoHS compliant】
 CAA572,CAA573 type
 COG Characteristics

Please return this specification to TDK representatives with your signature.
 If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

RECEIPT CONFIRMATION

DATE: YEAR MONTH DAY

TDK Corporation
 Sales
 Electronic Components
 Sales & Marketing Group

Engineering
 Electronic Components Business Company
 Ceramic Capacitors Business Group

APPROVED	Person in charge

APPROVED	CHECKED	Person in charge

SCOPE

This delivery specification shall be applied to Multilayer ceramic chip capacitors (Mega cap CA series) to be delivered to _____.

PRODUCTION PLACES

Production places defined in this specification shall be TDK Corporation, TDK Xiamen Co.,Ltd, TDK(Suzhou)Co.,Ltd and TDK Components U.S.A.Inc.

PRODUCT NAME

The name of the product to be defined in this specifications shall be CAA57◇○○○△△□□×.

REFERENCE STANDARD

JIS C 5101-1 : 2010	Fixed capacitors for use in electronic equipment-Part 1: Generic specification
C 5101-21 : 2014	Fixed capacitors for use in electronic equipment-Part 21 : Sectional specification : Fixed surface mount multilayer capacitors of ceramic dielectric,Class1
C 0806-3 : 2014	Packaging of components for automatic handling - Part 3 : Packaging of surface mount components on continuous tapes
JEITA RCR-2335 C 2014	Safety application guide for fixed ceramic capacitors for use in electronic equipment

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EXPLANATORY NOTE

When the mistrust in the spec arises, this specification is given priority. And it will be confirmed by written spec change after conference of both posts involved.

This specification warrants the quality of the ceramic chip capacitor. Capacitors should be evaluated or confirmed a state of mounted on your product.

If the use of the capacitors goes beyond the bounds of this specification, we can not afford to guarantee.

Division	Date	SPEC. No.
Ceramic Capacitors Business Group	April., 2022	C-LMEGA-C-g

1. CODE CONSTRUCTION

(Example) CA A 57 2 C0G 3A 303 J T OOOO
CA A 57 3 C0G 2J 304 J T OOOO
 (1) (2) (3) (4) (5) (6) (7) (8) (9) (10)

(1) Series

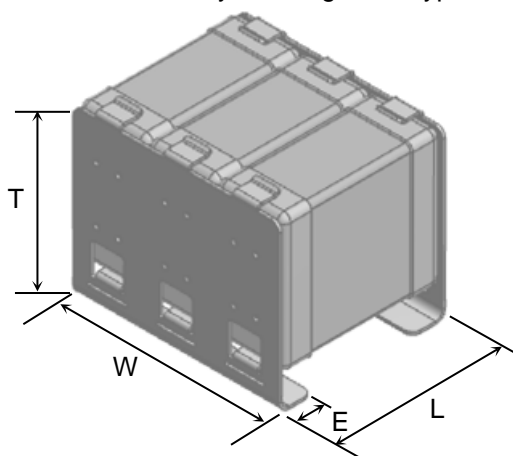
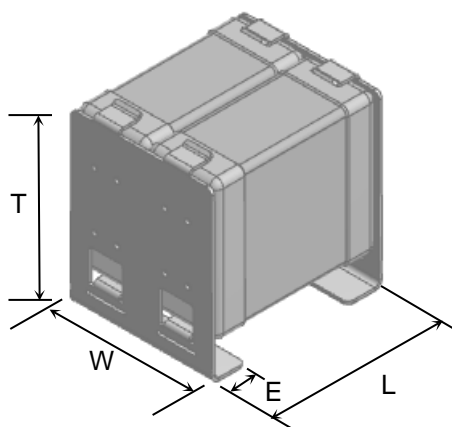
Symbol	Series
CA	Mega cap CA series

(2) TDK's auxiliary code

(3) Type

CAA572 : 2 side-by-side alignment type

CAA573 : 3 side-by-side alignment type



Type	Structure Symbol	Dimensions (Unit : mm)			
		L	W	T	E
57	2	6.00±0.50	5.60±0.50	6.40±0.50	1.20±0.20
57	3	6.00±0.50	8.40±0.50	6.40±0.50	1.20±0.20

*As for each item, please refer to to detail page on TDK web.

(4) Structure

Symbol	Structure
2	2 side-by-side alignment type
3	3 side-by-side alignment type

(5) Temperature Characteristics

Symbol	Temperature Characteristics
C0G	0 ± 30 ppm/°C (-55 ~ 125°C)

(6) Rated Voltage

Symbol	Rated Voltage
3 A	DC 1 kV
2 J	DC 630 V

(7) Rated Capacitance

Stated in three digits and in units of pico farads (pF).
The first and second digits identify the first and second significant figures of the Capacitance, the third digit identifies the multiplier.

(Example)

Symbol	Rated Capacitance
303	30,000 pF
304	300,000 pF

(8) Capacitance tolerance

Symbol	Tolerance
J	± 5 %

(9) Packaging

Symbol	Packaging
T	Taping

(10) TDK internal code

2. OPERATING TEMPERATURE RANGE

Min. operating Temperature	Max. operating Temperature	Reference Temperature
-55°C	125°C	25°C

3. STORING CONDITION AND TERM

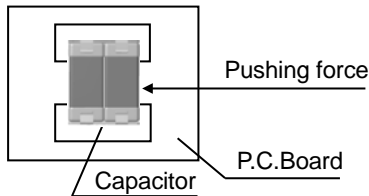
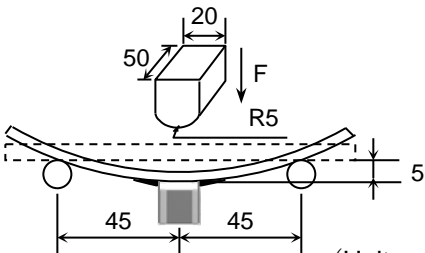
Storing temperature	Storing humidity	Storing term
5~40°C	20~70%RH	Within 6 months upon receipt.

4. INDUSTRIAL WASTE DISPOSAL

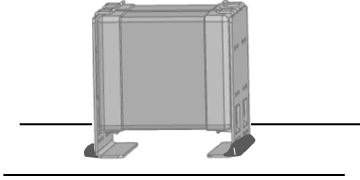
Dispose this product as industrial waste in accordance with the Industrial Waste Law.

5. PERFORMANCE

Table 1

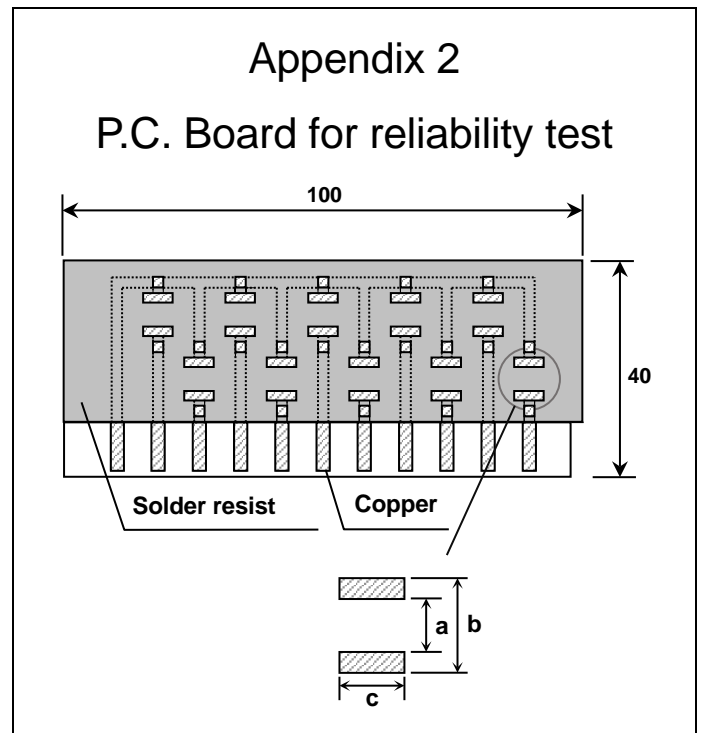
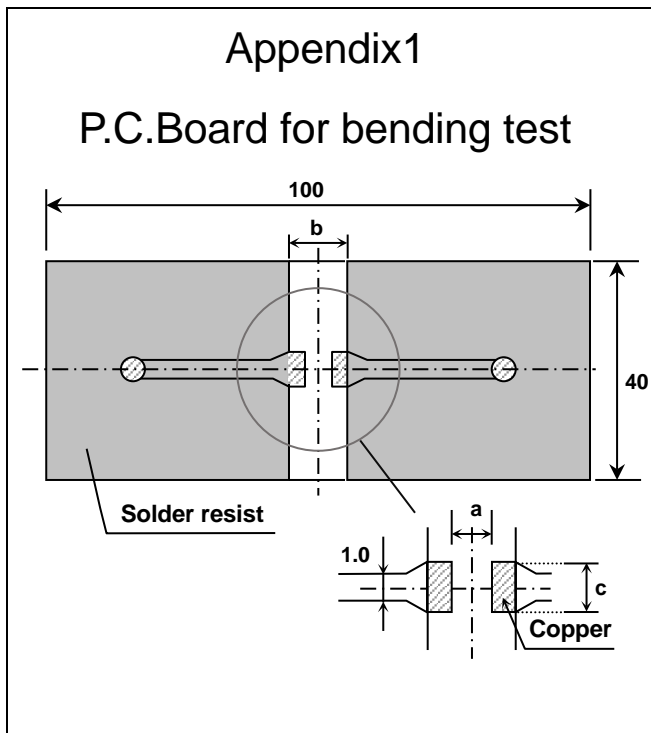
No.	Item	Performance	Test or inspection method								
1	External Appearance	No defects which may affect performance.	Inspect with magnifying glass(3×)								
2	Insulation Resistance	10,000MΩ or 500MΩ · μF min., whichever smaller.	Measuring voltage : 500V DC. Voltage application time : 60s.								
3	Voltage Proof	Withstand test voltage without insulation breakdown or other damage.	<table border="1"> <thead> <tr> <th>Rated voltage(RV)</th> <th>Apply voltage</th> </tr> </thead> <tbody> <tr> <td>630V</td> <td>1.3 × rated voltage</td> </tr> <tr> <td>1kV</td> <td>1.2 × rated voltage</td> </tr> </tbody> </table> Voltage application time : 1s. Charge / discharge current : 50mA or lower	Rated voltage(RV)	Apply voltage	630V	1.3 × rated voltage	1kV	1.2 × rated voltage		
Rated voltage(RV)	Apply voltage										
630V	1.3 × rated voltage										
1kV	1.2 × rated voltage										
4	Capacitance	Within the specified tolerance.	<table border="1"> <thead> <tr> <th>Measuring frequency</th> <th>Measuring voltage</th> </tr> </thead> <tbody> <tr> <td>1kHz±10%</td> <td>0.5 ~ 5V rms.</td> </tr> </tbody> </table>	Measuring frequency	Measuring voltage	1kHz±10%	0.5 ~ 5V rms.				
Measuring frequency	Measuring voltage										
1kHz±10%	0.5 ~ 5V rms.										
5	Q	Please refer to detail page on TDK web.	See No.4 in this table for measuring condition.								
6	Temperature Characteristics of Capacitance	<table border="1"> <thead> <tr> <th>T.C.</th> <th>Temperature Coefficient (ppm/°C)</th> </tr> </thead> <tbody> <tr> <td>COG</td> <td>0 ± 30</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Capacitance drift</th> <th>Within ± 0.2%</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> </tr> </tbody> </table>	T.C.	Temperature Coefficient (ppm/°C)	COG	0 ± 30	Capacitance drift	Within ± 0.2%			Temperature coefficient shall be calculated based on values at 25°C and 85°C temperature. Measuring temperature below 25°C shall be -10°C and -25°C.
T.C.	Temperature Coefficient (ppm/°C)										
COG	0 ± 30										
Capacitance drift	Within ± 0.2%										
7	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.	Reflow solder the capacitors on a P.C.Board shown in Appendix 2. Apply a pushing force gradually at the center of a specimen in a horizontal direction of P.C.board. Pushing force : 5N Holding time : 10±1s 								
8	Bending	External appearance	No mechanical damage. Reflow solder the capacitor on a P.C.Board shown in Appendix 1.  (Unit : mm)								

(continued)

No.	Item	Performance	Test or inspection method																				
9	Solderability	<p>Both end faces and the contact are as shall be covered with a smooth and bright solder coating with no more than a small amount of scattered imperfections such as pinholes or un-wetted or de-wetted areas. These imperfections shall not be concentrated in one area.</p> 	<p>Solder : Sn-3.0Ag-0.5Cu</p> <p>Reflow solder the capacitor on a P.C.Board shown in Appendix2.</p> <p>Please refer to No.5 Soldering in 10.CAUTION for soldering condition.</p>																				
10	Vibration	<p>External appearance</p> <p>Capacitance</p> <table border="1" data-bbox="528 808 935 943"> <thead> <tr> <th>Characteristics</th> <th>Change from the value before test</th> </tr> </thead> <tbody> <tr> <td>C0G</td> <td>± 2.5 %</td> </tr> </tbody> </table> <p>Q</p>	Characteristics	Change from the value before test	C0G	± 2.5 %	<p>No mechanical damage.</p> <p>1,000 min.</p>	<p>Frequency : 10~55~10Hz</p> <p>Reciprocating sweep time : 1 min.</p> <p>Amplitude : 1.5mm</p> <p>Repeat this for 2h each in 3 perpendicular directions(Total 6h).</p> <p>Reflow solder the capacitors on a P.C.Board shown in Appendix 2 before testing.</p>															
Characteristics	Change from the value before test																						
C0G	± 2.5 %																						
11	Temperature Cycle	<p>External appearance</p> <p>Capacitance</p> <table border="1" data-bbox="528 1211 935 1379"> <thead> <tr> <th>Characteristics</th> <th>Change from the value before test</th> </tr> </thead> <tbody> <tr> <td>C0G</td> <td>Please contact with our sales representative.</td> </tr> </tbody> </table> <p>Q</p> <p>Insulation Resistance</p> <p>Voltage proof</p>	Characteristics	Change from the value before test	C0G	Please contact with our sales representative.	<p>No mechanical damage.</p> <p>1,000 min.</p> <p>Meet the initial spec.</p> <p>No insulation breakdown or other damage.</p>	<p>Expose the capacitors in the condition step1 through step 4 listed in the following table.</p> <p>Temp. cycle : 100 cycles</p> <table border="1" data-bbox="991 1301 1430 1547"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> <th>Time(min.)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>-55 ± 3</td> <td>30±3</td> </tr> <tr> <td>2</td> <td>Ambient Temp.</td> <td>2 ~ 5</td> </tr> <tr> <td>3</td> <td>125 ± 2</td> <td>30±2</td> </tr> <tr> <td>4</td> <td>Ambient Temp.</td> <td>2 ~ 5</td> </tr> </tbody> </table> <p>Leave the capacitors in ambient condition for 6~24h before measurement.</p> <p>Reflow solder the capacitors on a P.C.Board shown in Appendix2 before testing.</p>	Step	Temperature(°C)	Time(min.)	1	-55 ± 3	30±3	2	Ambient Temp.	2 ~ 5	3	125 ± 2	30±2	4	Ambient Temp.	2 ~ 5
Characteristics	Change from the value before test																						
C0G	Please contact with our sales representative.																						
Step	Temperature(°C)	Time(min.)																					
1	-55 ± 3	30±3																					
2	Ambient Temp.	2 ~ 5																					
3	125 ± 2	30±2																					
4	Ambient Temp.	2 ~ 5																					

(continued)

No.	Item		Performance	Test or inspection method	
12	Moisture Resistance (Steady State)	External appearance	No mechanical damage.	Test temp. : $40\pm 2^{\circ}\text{C}$ Test humidity : 90~95%RH Test time : 500 +24,0h Leave the capacitors in ambient condition for 6~24h before measurement. Reflow solder the capacitors on a P.C.Board shown in Appendix2 before testing.	
		Capacitance	Characteristics		Change from the value before test
			COG		Please contact with our sales representative.
		Q	350 min.		
Insulation Resistance	1,000M Ω or 50M Ω · μF min., whichever smaller.				
13	Life	External appearance	No mechanical damage.	Test temp. : $125\pm 2^{\circ}\text{C}$ Applied voltage : Rated voltage Test time : 1,000 +48,0h Charge/discharge current : 50mA or lower Leave the capacitors in ambient condition for 6~24h before measurement. Reflow solder the capacitors on a P.C.Board shown in Appendix2 before testing.	
		Capacitance	Characteristics		Change from the value before test
			COG		Please contact with our sales representative.
		Q	350 min.		
Insulation Resistance	1,000M Ω or 50M Ω · μF min., whichever smaller.				



(Unit : mm)

Type	Dimensions		
TDK(EIA style)	a	b	c
CAA572	4.5	8.0	5.6
CAA573	4.5	8.0	8.1

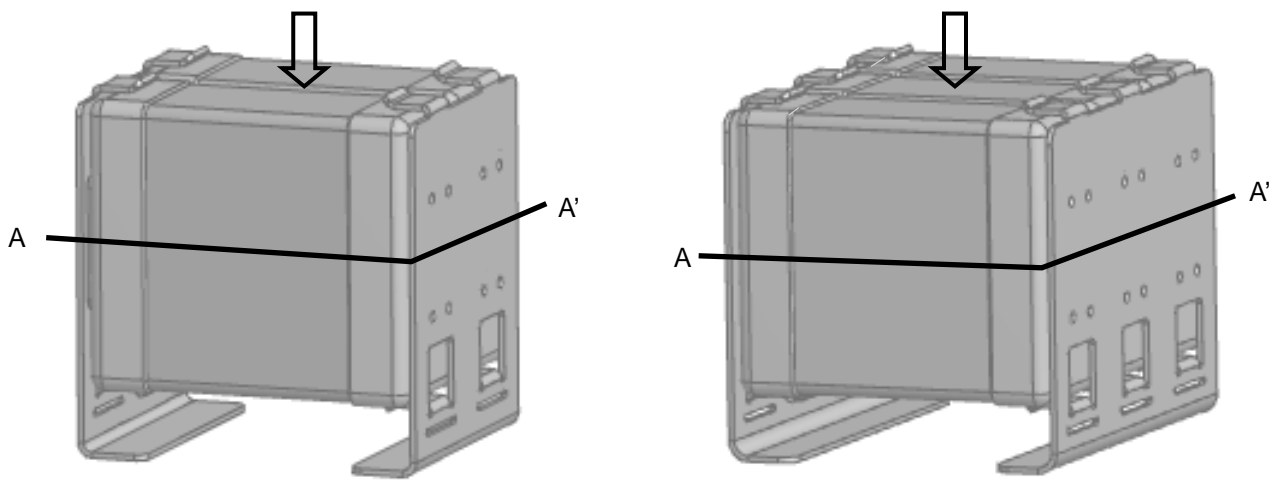
1. Material : Glass Epoxy(As per JIS C6484 GE4)

2. Thickness : 1.6mm

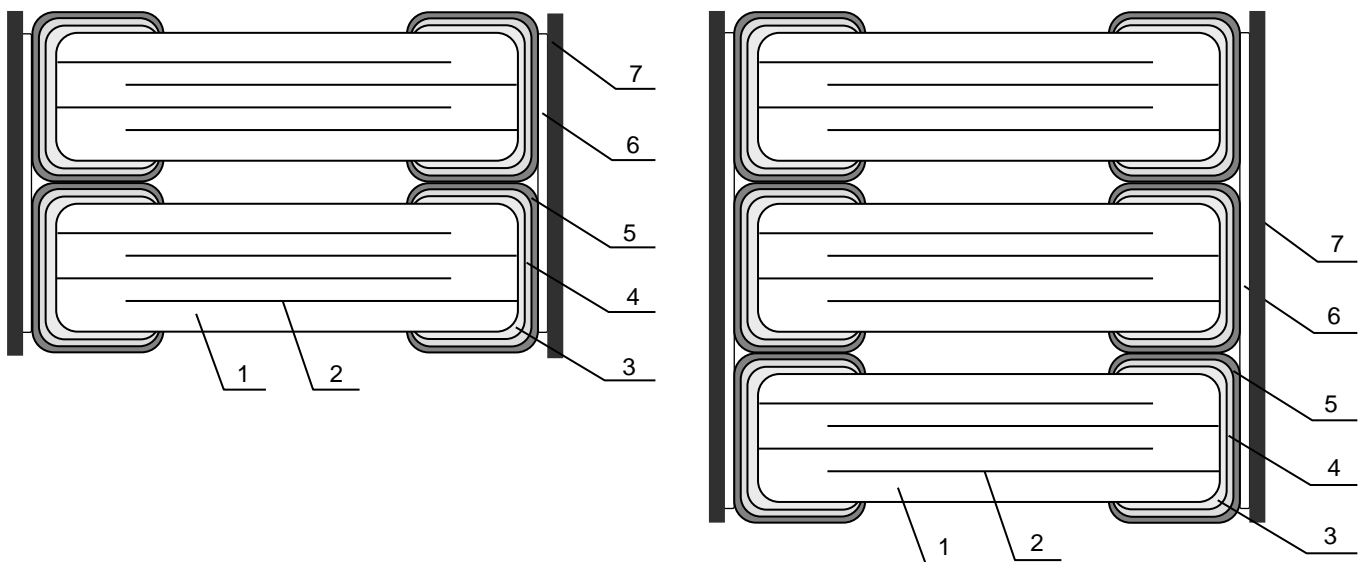
 Copper(Thickness:0.035mm)

 Solder resist

6. INSIDE STRUCTURE AND MATERIAL



A-A'



No.	NAME	MATERIAL
1	Dielectric	CaZrO ₃
2	Electrode	Nickel (Ni)
3	Termination	Copper (Cu)
4		Nickel (Ni)
5		Tin (Sn)
6	Metal cap joint	High temp solder
7	Metal cap	Clad

7. PACKAGING

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

Tape packaging is as per 11. TAPE PACKAGING SPECIFICATION.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

*Composition of Inspection No.

Example F 2 A - 23 - 001
 (a) (b) (c) (d) (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

*Composition of new Inspection No.

(Will be implemented on and after May. 1, 2019)

Example

I	F	2	E	2	3	A	0	0	1
(a)	(b)	(c)	(d)	(e)	(f)	(g)			

- (a) Prefix
- (b) Line code
- (c) Last digit of the year
- (d) Month and A for January and B for February and so on. (Skip I)
- (e) Inspection Date of the month.
- (f) Serial No. of the day(00 ~ ZZ)
- (g) Suffix(00 ~ ZZ)

* It was shifted to the new inspection No. on and after May 2019, but the implementation timing may be different depending on shipment bases. Until the shift is completed, either current or new composition of inspection No. will be applied.

8. RECOMMENDATION

It is recommended to provide a slit (about 1mm wide) in the board under the components to improve washing Flux.


And please make sure to dry detergent up completely before.


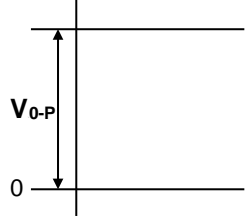
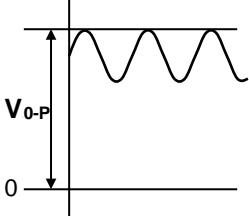
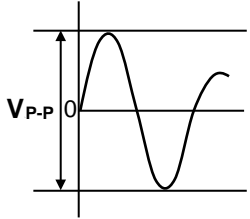
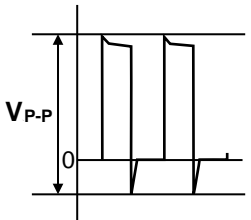
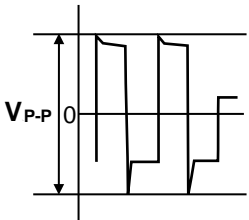
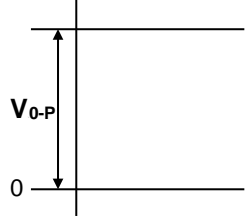
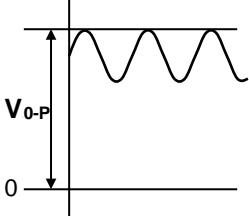
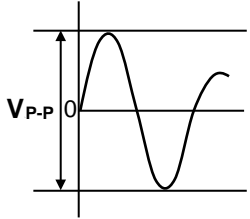
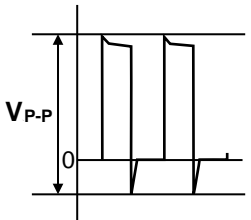
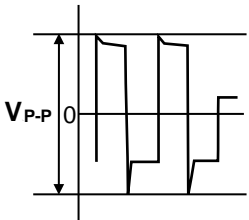
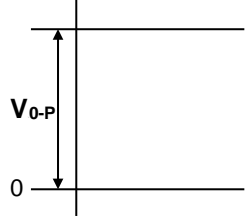
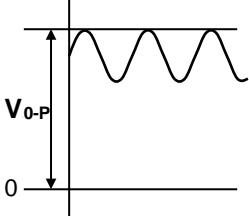
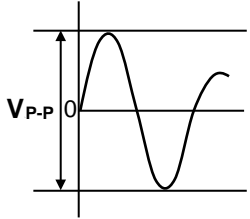
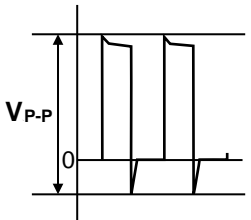
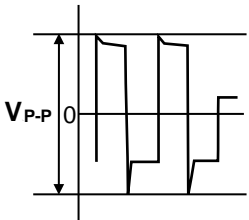
9. SOLDERING CONDITION

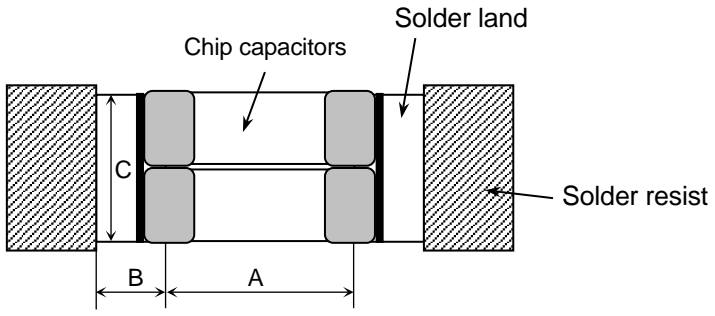
Reflow soldering only.

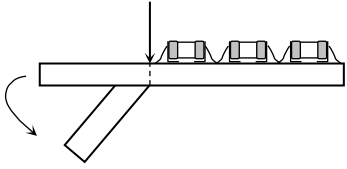
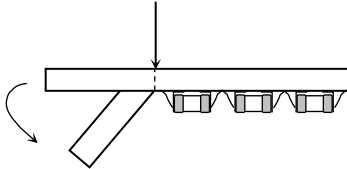
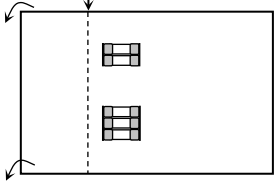
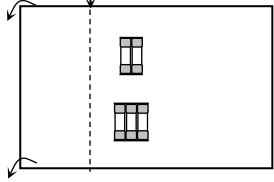
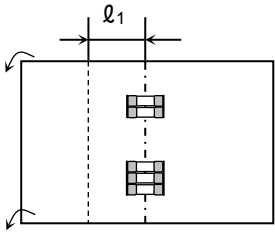
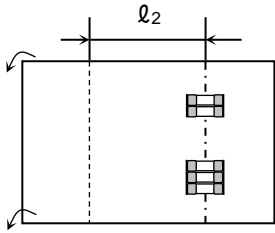
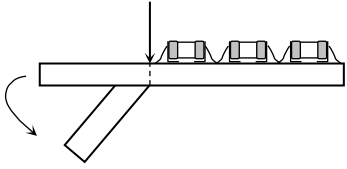
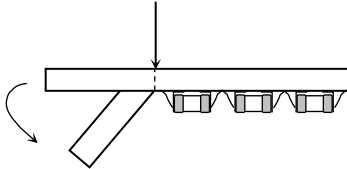
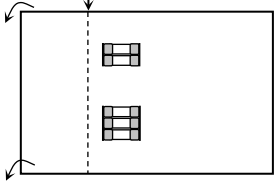
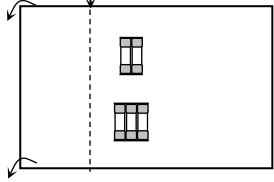
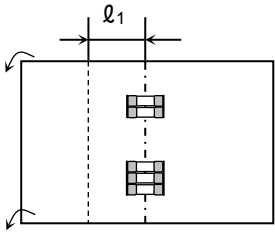
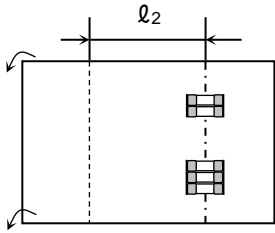
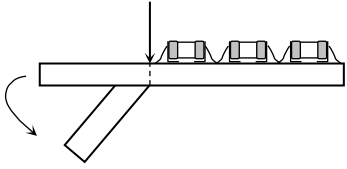
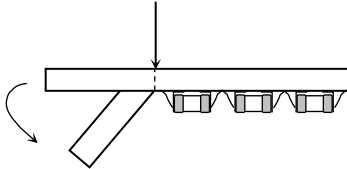
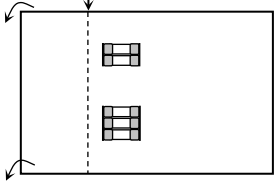
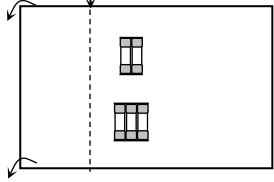
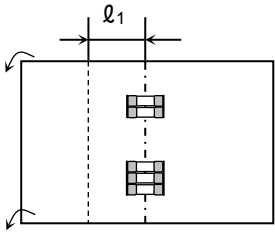
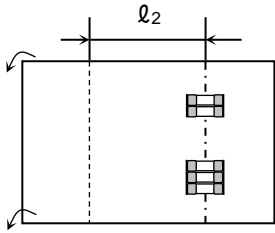
Please refer to No.5 Soldering in 10. CAUTION for recommended soldering condition.

10. CAUTION

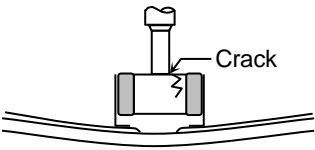
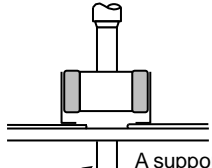
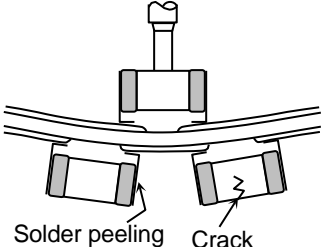
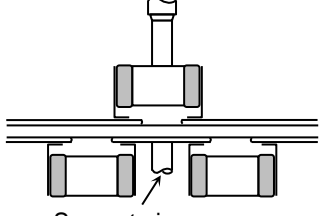
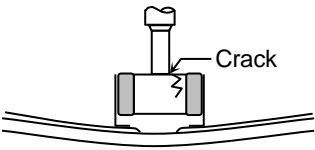
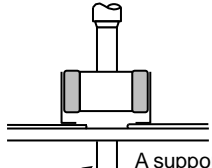
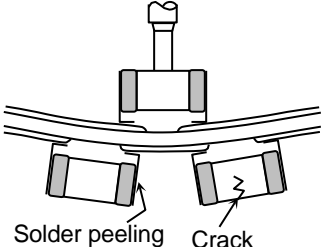
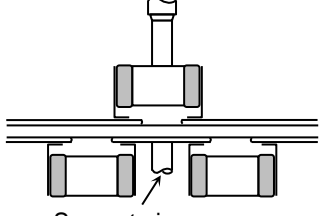
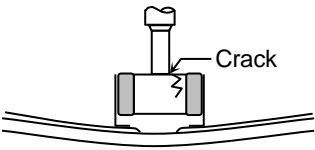
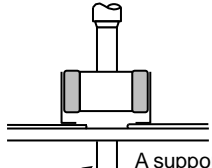
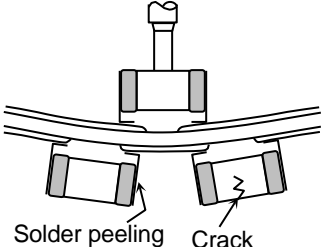
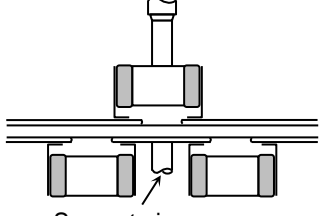
No.	Process	Condition
1	Operating Condition (Storage, Use, Transportation)	<p>1-1. Storage, Use The capacitors must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. JIS C 60721-3-1 Class 1K2 should be followed for the other climatic conditions.</p> <ol style="list-style-type: none"> 1) High temperature and humidity environment may affect a capacitor's solder ability because it accelerates terminal oxidization. They also deteriorate performance of taping and packaging. Therefore, SMD capacitors shall be used within 6 months. For capacitors with terminal electrodes consisting of silver or silver-palladium which tend to become oxidized or sulfurized, use as soon as possible, such as within one month after opening the bag. 2) When capacitors are stored for a period longer than specified, confirm the solderability of the capacitors prior to use. During storage, keep the minimum packaging unit in its original packaging without opening it. Do not deviate from the above temperature and humidity conditions even for a short term. 3) Corrosive gasses in the air or atmosphere may result in deterioration of the reliability, such as poor solderability of the terminal electrodes. Do not store capacitors where they will be exposed to corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine ammonia etc.) 4) Solderability and electrical performance may deteriorate due to photochemical change in the terminal electrode if stored in direct sunlight, or due to condensation from rapid changes in humidity. The capacitors especially which use resin material must be operated and stored in an environment free of dew condensation, as moisture absorption due to condensation may affect the performance. 5) Refer to JIS C 60721-3-1, class 1K2 for other climate conditions. <p>1-2. Handling in transportation In case of the transportation of the capacitors, the performance of the capacitors may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335C 9.2 Handling in transportation)</p>
2	Circuit design  Caution	<p>2-1. Operating temperature</p> <ol style="list-style-type: none"> 1) Upper category temperature (maximum operating temperature) is specified. It is necessary to select a capacitor whose rated temperature is higher than the operating temperature. Also, it is necessary to consider the temperature distribution in the equipment and seasonal temperature variation. 2) Surface temperature including self heating should be below maximum operating temperature. Due to dielectric loss, capacitors will heat itself when AC is applied due to ESR. Especially at high frequencies, please be careful that the heat might be so extreme. Also, even if the surface temperature of the capacitor includes self-heating and is the maximum operating temperature or lower, excessive heating of the capacitor due to self-heating may cause deterioration of the characteristics and reliability of the capacitor. The self-heating temperature rise of the capacitor changes depending on the difference in heat radiation due to the mounting method to the device, the ambient temperature, the cooling method of the device, etc. As a guide, please consult us if the self-heating temperature rise of the capacitor in a natural convection environment at an ambient temperature of 25°C exceeds 5°C. When using in a high-frequency circuit or a circuit in which a capacitor generates heat, such as when a high-frequency ripple current flows, pay attention to the above precautions. (Note that accurate measurement may not be possible with self-heating measurement when the equipment applies cooling other than natural convection such as a cooling fan.) 3) The electrical characteristics of the capacitors will vary depending on the temperature. The capacitors should be selected and designed in taking the temperature into consideration.

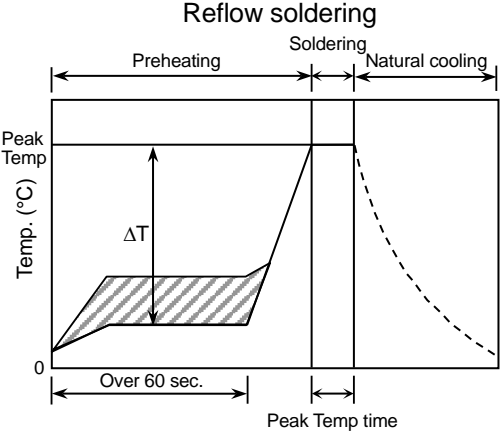
No.	Process	Condition														
2	Circuit design  Caution	<p>2-2. When overvoltage is applied Applying overvoltage to a capacitor may cause dielectric breakdown and result in a short circuit. The duration until dielectric breakdown depends on the applied voltage and the ambient temperature.</p> <p>2-3. Operating voltage</p> <p>1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. — (1) and (2) AC or pulse with overshooting, V_{P-P} must be below the rated voltage. — (3), (4) and (5)</p> <p>When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitors within rated voltage containing these Irregular voltage.</p> <table border="1" data-bbox="475 667 1449 1243"> <thead> <tr> <th data-bbox="475 667 667 712">Voltage</th> <th data-bbox="667 667 927 712">(1) DC voltage</th> <th data-bbox="927 667 1187 712">(2) DC+AC voltage</th> <th data-bbox="1187 667 1449 712">(3) AC voltage</th> </tr> </thead> <tbody> <tr> <td data-bbox="475 712 667 943">Positional Measurement (Rated voltage)</td> <td data-bbox="667 712 927 943">  </td> <td data-bbox="927 712 1187 943">  </td> <td data-bbox="1187 712 1449 943">  </td> </tr> <tr> <th data-bbox="475 965 667 1010">Voltage</th> <th data-bbox="667 965 927 1010">(4) Pulse voltage (A)</th> <th data-bbox="927 965 1187 1010">(5) Pulse voltage (B)</th> </tr> <tr> <td data-bbox="475 1010 667 1243">Positional Measurement (Rated voltage)</td> <td data-bbox="667 1010 927 1243">  </td> <td data-bbox="927 1010 1187 1243">  </td> </tr> </tbody> </table> <p>2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitors may be reduced.</p> <p>3) The effective capacitance will vary depending on applied DC and AC voltages. The capacitors should be selected and designed in taking the voltages into consideration.</p> <p>4) Abnormal voltage (surge voltage, static electricity, pulse voltage, etc.) shall not exceed the rated voltage.</p> <p>5) When capacitors are used in a series connection, it is necessary to add a balancing circuit such as voltage dividing resistors in order to avoid an imbalance in the voltage applied to each capacitor.</p>	Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage	Positional Measurement (Rated voltage)				Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)	Positional Measurement (Rated voltage)		
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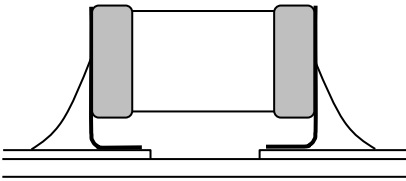
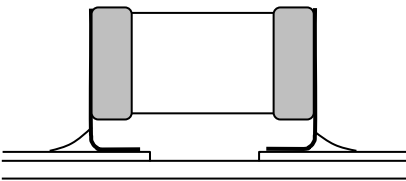
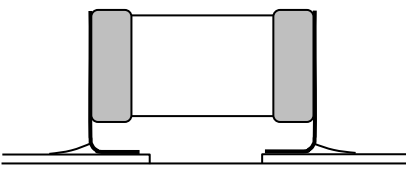
No.	Process	Condition												
3	Designing P.C.board	<p>The amount of solder at the terminations has a direct effect on the reliability of the capacitor.</p> <ol style="list-style-type: none"> 1) The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the terminations. 2) Avoid using common solder land for multiple terminations and provide individual solder land for each terminations. 3) Size and recommended land dimensions. <div style="text-align: center;">  </div> <div style="text-align: right; margin-right: 100px;">(Unit : mm)</div> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">Case size Symbol</th> <th style="text-align: center;">CAA572</th> <th style="text-align: center;">CAA573</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">4.3 ~ 4.7</td> <td style="text-align: center;">4.3 ~ 4.7</td> </tr> <tr> <td style="text-align: center;">B</td> <td style="text-align: center;">1.5 ~ 2.0</td> <td style="text-align: center;">1.5 ~ 2.0</td> </tr> <tr> <td style="text-align: center;">C</td> <td style="text-align: center;">5.2 ~ 5.7</td> <td style="text-align: center;">7.9 ~ 8.4</td> </tr> </tbody> </table>	Case size Symbol	CAA572	CAA573	A	4.3 ~ 4.7	4.3 ~ 4.7	B	1.5 ~ 2.0	1.5 ~ 2.0	C	5.2 ~ 5.7	7.9 ~ 8.4
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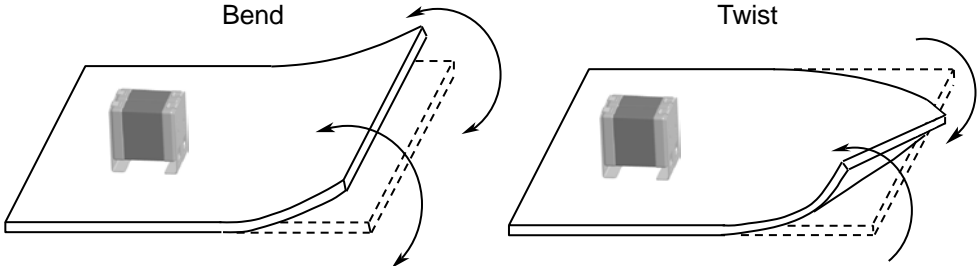
No.	Process	Condition												
3	Designing P.C.board	<p data-bbox="432 215 1091 248">4) Recommended chip capacitor layout is as following.</p> <table border="1" data-bbox="472 331 1417 1751"> <thead> <tr> <th data-bbox="472 331 643 409"></th> <th data-bbox="643 331 1031 409">Disadvantage against bending stress</th> <th data-bbox="1031 331 1417 409">Advantage against bending stress</th> </tr> </thead> <tbody> <tr> <td data-bbox="472 409 643 824">Mounting face</td> <td data-bbox="643 409 1031 824"> <p data-bbox="735 454 938 488">Perforation or slit</p>  <p data-bbox="679 678 932 745">Break P.C.board with mounted side up.</p> </td> <td data-bbox="1031 409 1417 824"> <p data-bbox="1123 454 1326 488">Perforation or slit</p>  <p data-bbox="1074 678 1326 745">Break P.C.board with mounted side down.</p> </td> </tr> <tr> <td data-bbox="472 824 643 1272">Chip arrangement (Direction)</td> <td data-bbox="643 824 1031 1272"> <p data-bbox="735 947 938 981">Perforation or slit</p>  </td> <td data-bbox="1031 824 1417 1272"> <p data-bbox="1123 947 1326 981">Perforation or slit</p>  </td> </tr> <tr> <td data-bbox="472 1272 643 1751">Distance from slit</td> <td data-bbox="643 1272 1031 1751"> <p data-bbox="671 1283 1002 1317">Closer to slit is higher stress</p>  <p data-bbox="855 1653 986 1686">$(l_1 < l_2)$</p> </td> <td data-bbox="1031 1272 1417 1751"> <p data-bbox="1054 1283 1385 1317">Away from slit is less stress</p>  <p data-bbox="1238 1653 1369 1686">$(l_1 < l_2)$</p> </td> </tr> </tbody> </table>		Disadvantage against bending stress	Advantage against bending stress	Mounting face	<p data-bbox="735 454 938 488">Perforation or slit</p>  <p data-bbox="679 678 932 745">Break P.C.board with mounted side up.</p>	<p data-bbox="1123 454 1326 488">Perforation or slit</p>  <p data-bbox="1074 678 1326 745">Break P.C.board with mounted side down.</p>	Chip arrangement (Direction)	<p data-bbox="735 947 938 981">Perforation or slit</p> 	<p data-bbox="1123 947 1326 981">Perforation or slit</p> 	Distance from slit	<p data-bbox="671 1283 1002 1317">Closer to slit is higher stress</p>  <p data-bbox="855 1653 986 1686">$(l_1 < l_2)$</p>	<p data-bbox="1054 1283 1385 1317">Away from slit is less stress</p>  <p data-bbox="1238 1653 1369 1686">$(l_1 < l_2)$</p>
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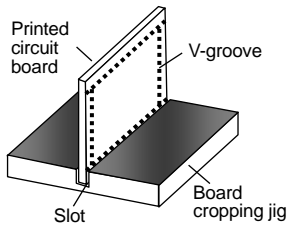
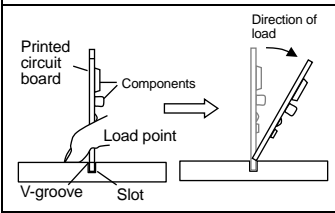
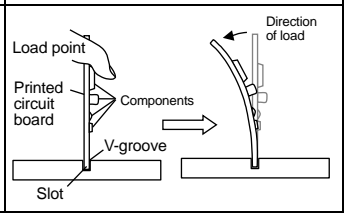
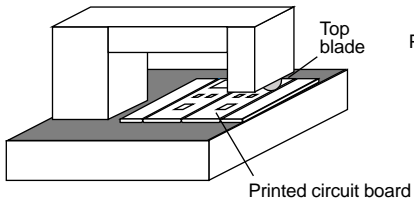
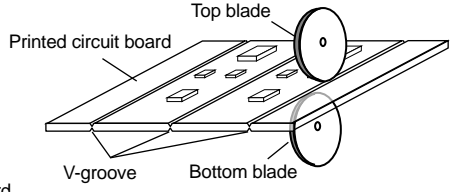
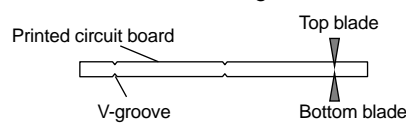
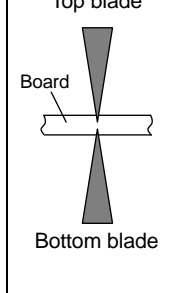
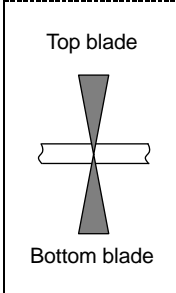
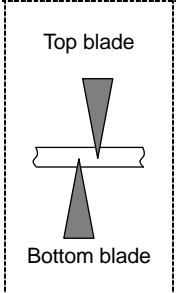
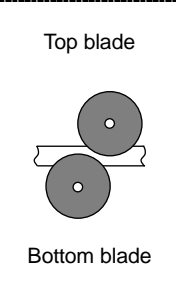
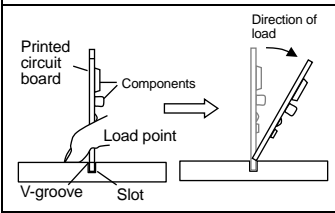
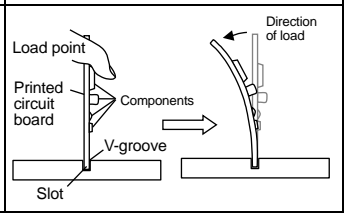
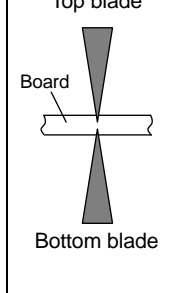
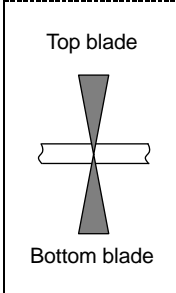
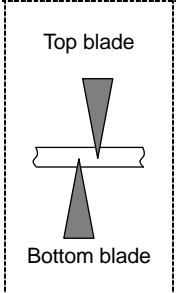
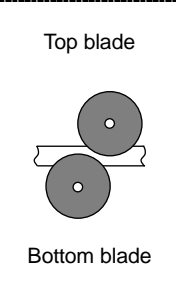
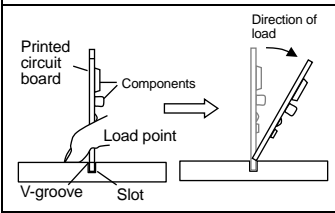
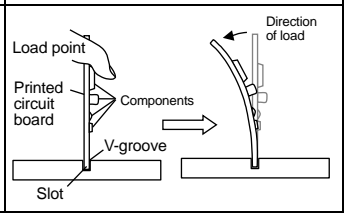
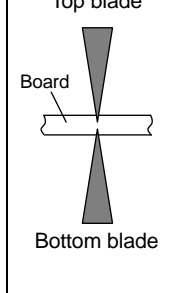
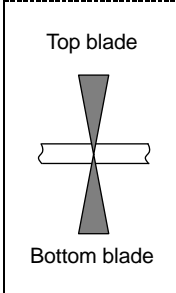
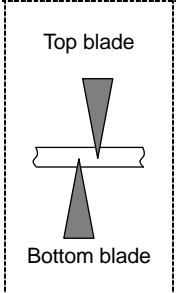
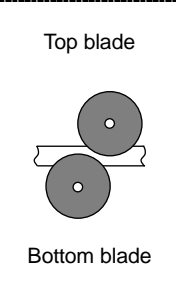
No.	Process	Condition												
3	Designing P.C.board	<p>5) Mechanical stress varies according to location of chip capacitors on the P.C.board.</p> <div data-bbox="411 291 1452 851" style="border: 1px solid black; padding: 10px;"> <p style="text-align: right;">Stress force $A > B > E$ $A > D > E$ $A > C$</p> </div> <p>When dividing printed wiring boards, the intensities of mechanical stress applied to capacitors are different according to each dividing method in the order of : Push-back < Slit < V-groove < Perforation. Therefore consider not only position of capacitors, but also the way of the dividing the printed wiring boards.</p> <p>6) Layout recommendation</p> <table border="1" data-bbox="411 1086 1484 2004"> <thead> <tr> <th data-bbox="411 1086 545 1205">Example</th> <th data-bbox="545 1086 849 1205">Use of common solder land</th> <th data-bbox="849 1086 1152 1205">Soldering with chassis</th> <th data-bbox="1152 1086 1484 1205">Use of common solder land with other SMD</th> </tr> </thead> <tbody> <tr> <td data-bbox="411 1205 545 1585">Need to avoid</td> <td data-bbox="545 1205 849 1585"> </td> <td data-bbox="849 1205 1152 1585"> </td> <td data-bbox="1152 1205 1484 1585"> </td> </tr> <tr> <td data-bbox="411 1585 545 2004">Recommendation</td> <td data-bbox="545 1585 849 2004"> </td> <td data-bbox="849 1585 1152 2004"> </td> <td data-bbox="1152 1585 1484 2004"> </td> </tr> </tbody> </table>	Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD	Need to avoid				Recommendation			
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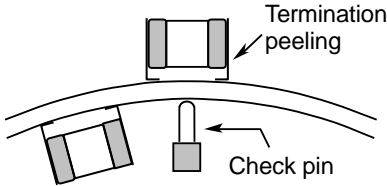
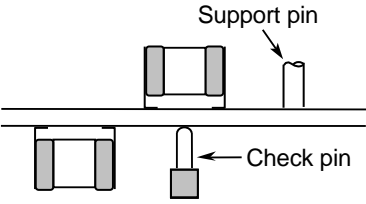
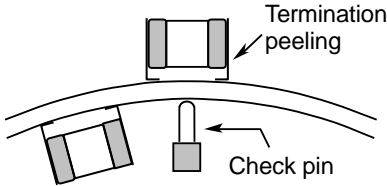
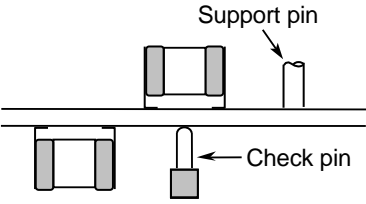
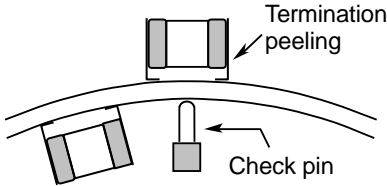
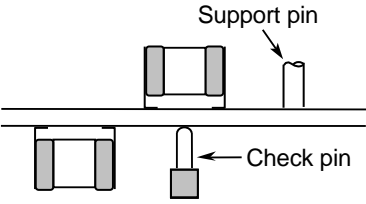
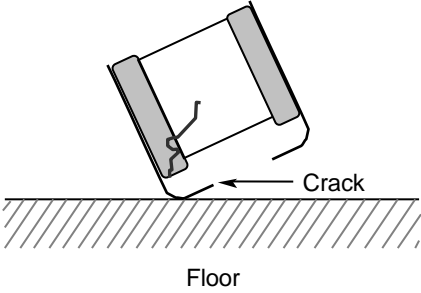
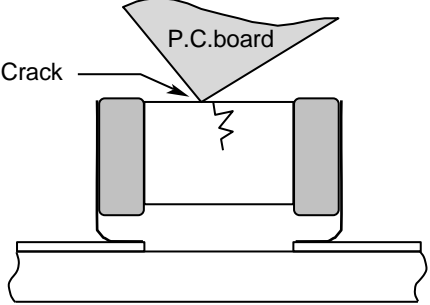
No.	Process	Condition									
4	Mounting	<p>4-1. Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitor to result in cracking. Please take following precautions.</p> <ol style="list-style-type: none"> 1) Adjust the bottom dead center of the mounting head to reach on the P.C.board surface and not press it. 2) Adjust the mounting head pressure to be 1 to 3N of static weight. 3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board. See following examples. <table border="1" data-bbox="485 640 1437 1245"> <thead> <tr> <th data-bbox="485 640 687 689"></th> <th data-bbox="687 640 1059 689">Not recommended</th> <th data-bbox="1059 640 1437 689">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="485 689 687 954">Single sided mounting</td> <td data-bbox="687 689 1059 954">  </td> <td data-bbox="1059 689 1437 954">  <p>A support pin is not to be underneath the capacitor.</p> </td> </tr> <tr> <td data-bbox="485 954 687 1245">Double-sides mounting</td> <td data-bbox="687 954 1059 1245">  </td> <td data-bbox="1059 954 1437 1245">  </td> </tr> </tbody> </table> <p>When the centering jaw is worn out, it may give mechanical impact on the capacitor to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.</p>		Not recommended	Recommended	Single sided mounting		 <p>A support pin is not to be underneath the capacitor.</p>	Double-sides mounting		
	Not recommended	Recommended									
Single sided mounting		 <p>A support pin is not to be underneath the capacitor.</p>									
Double-sides mounting											


No.	Process	Condition															
5	Soldering	<p>5-1. Flux selection Flux can seriously affect the performance of capacitors. Confirm the following to select the appropriate flux.</p> <ol style="list-style-type: none"> 1) It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended. 2) Excessive flux must be avoided. Please provide proper amount of flux. 3) When water-soluble flux is used, enough washing is necessary. <p>5-2. Recommended Reflow soldering profile</p> <ol style="list-style-type: none"> 1) Soldering condition (Preheating temperature, soldering temperature and these times) is limited to reflow soldering method which is stipulated on the specification. 2) Chips should be mounted, shortly after a solder is on a P.C.Board. <div style="text-align: center;"> <p>Reflow soldering</p>  </div> <p>5-3. Recommended soldering peak temp and peak temp duration Pb free solder is recommended, but if Sn-37Pb must be used, refer to below.</p> <table border="1" data-bbox="502 1332 1209 1518"> <thead> <tr> <th rowspan="2">Temp./Duration</th> <th colspan="2">Reflow soldering</th> </tr> <tr> <th>Peak temp(°C)</th> <th>Duration(sec.)</th> </tr> </thead> <tbody> <tr> <td>Lead Free Solder</td> <td>260 max.</td> <td>10 max.</td> </tr> <tr> <td>Sn-Pb Solder</td> <td>230 max.</td> <td>20 max.</td> </tr> </tbody> </table> <p>* 1 time reflow is recommended. Please inquire when reflow more than 2 times.</p> <p>Recommended solder compositions Lead Free Solder : Sn-3.0Ag-0.5Cu</p> <p>5-4. Avoiding thermal shock</p> <ol style="list-style-type: none"> 1) Preheating condition <table border="1" data-bbox="539 1792 997 1899"> <thead> <tr> <th>Soldering</th> <th>Temp. (°C)</th> </tr> </thead> <tbody> <tr> <td>Reflow soldering</td> <td>$\Delta T \leq 130$</td> </tr> </tbody> </table> 2) Cooling condition Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C. 	Temp./Duration	Reflow soldering		Peak temp(°C)	Duration(sec.)	Lead Free Solder	260 max.	10 max.	Sn-Pb Solder	230 max.	20 max.	Soldering	Temp. (°C)	Reflow soldering	$\Delta T \leq 130$
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No.	Process	Condition
5	Soldering	<p data-bbox="438 208 1465 320">5-5. Amount of solder Excessive solder will induce higher tensile force in chip capacitor when temperature changes and it may result in chip cracking. In sufficient solder may detach the capacitor from the P.C.board.</p> <hr/> <div data-bbox="499 376 1428 555"> <p data-bbox="499 427 619 483">Excessive solder</p>  <p data-bbox="1114 427 1428 483">Higher tensile force in chip capacitor to cause crack</p> </div> <hr/> <div data-bbox="499 600 1085 779"> <p data-bbox="499 667 619 701">Adequate</p>  </div> <hr/> <div data-bbox="499 824 1436 1003"> <p data-bbox="499 880 627 936">Insufficient solder</p>  <p data-bbox="1114 846 1436 969">Low robustness may cause contact failure or chip capacitor comes off the P.C.board.</p> </div> <hr/> <p data-bbox="438 1093 1145 1193">5-6. Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder.</p> <p data-bbox="438 1227 1465 1440">5-7. Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335C Annex A (Informative) Recommendations to prevent the tombstone phenomenon)</p> <p data-bbox="438 1507 1273 1608">5-8. Other notes related to soldering Do not reuse products that have been removed with a soldering iron. Also, mounting this product with a soldering iron is not guaranteed.</p>

No.	Process	Condition
6	Cleaning	<p>1) If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitor surface to deteriorate especially the insulation resistance.</p> <p>2) If cleaning condition is not suitable, it may damage the chip capacitor.</p> <p>2)-1. Insufficient washing</p> <p>(1) Terminal electrodes may corrode by Halogen in the flux.</p> <p>(2) Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance.</p> <p>(3) Water soluble flux has higher tendency to have above mentioned problems (1) and (2).</p> <p>2)-2. Excessive washing</p> <p>When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition.</p> <p style="padding-left: 40px;">Power : 20W/ℓ max. Frequency : 40kHz max. Washing time : 5 minutes max.</p> <p>2)-3. If the cleaning fluid is contaminated, density of Halogen increases, and it may bring the same result as insufficient cleaning.</p>
7	Coating and molding of the P.C.board	<p>1) When the P.C.board is coated, please verify the quality influence on the product.</p> <p>2) Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor.</p> <p>3) Please verify the curing temperature.</p>
8	Handling after chip mounted  Caution	<p>1) Please pay attention not to bend or distort the P.C.board after soldering in handling otherwise the chip capacitor may crack.</p> <div style="text-align: center;">  </div>

No.	Process	Condition																
8	Handling after chip mounted  Caution	<p>2) Printed circuit board cropping should not be carried out by hand, but by using the proper tooling. Printed circuit board cropping should be carried out using a board cropping jig as shown in the following figure or a board cropping apparatus to prevent inducing mechanical stress on the board.</p> <p>(1) Example of a board cropping jig</p> <p>Recommended example: The board should be pushed from the back side, close to the cropping jig so that the board is not bent and the stress applied to the capacitor is compressive.</p> <p>Unrecommended example: If the pushing point is far from the cropping jig and the pushing direction is from the front side of the board, large tensile stress is applied to the capacitor, which may cause cracks.</p> <div style="display: flex; justify-content: space-around;"> <div data-bbox="459 577 746 840"> <p>Outline of jig</p>  </div> <div data-bbox="762 571 1444 833"> <table border="1"> <thead> <tr> <th data-bbox="762 571 1098 622">Recommended</th> <th data-bbox="1098 571 1444 622">Unrecommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="762 622 1098 833">  </td> <td data-bbox="1098 622 1444 833">  </td> </tr> </tbody> </table> </div> </div> <p>(2) Example of a board cropping machine</p> <p>An outline of a printed circuit board cropping machine is shown below. The top and bottom blades are aligned with one another along the lines with the V-grooves on printed circuit board when cropping the board.</p> <p>Unrecommended example: Misalignment of blade position between top and bottom, right and left, or front and rear blades may cause a crack in the capacitor.</p> <div style="display: flex; justify-content: space-around;"> <div data-bbox="555 1146 970 1411"> <p>Outline of machine</p>  </div> <div data-bbox="957 1146 1412 1400"> <p>Principle of operation</p>  </div> </div> <div style="text-align: center; margin: 10px 0;"> <p>Cross-section diagram</p>  </div> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th data-bbox="638 1624 821 1713">Recommended</th> <th colspan="3" data-bbox="821 1624 1348 1668">Unrecommended</th> </tr> <tr> <td></td> <th data-bbox="821 1668 997 1758">Top-bottom misalignment</th> <th data-bbox="997 1668 1173 1758">Left-right misalignment</th> <th data-bbox="1173 1668 1348 1758">Front-rear misalignment</th> </tr> </thead> <tbody> <tr> <td data-bbox="638 1758 821 2049">  </td> <td data-bbox="821 1758 997 2049">  </td> <td data-bbox="997 1758 1173 2049">  </td> <td data-bbox="1173 1758 1348 2049">  </td> </tr> </tbody> </table>	Recommended	Unrecommended			Recommended	Unrecommended				Top-bottom misalignment	Left-right misalignment	Front-rear misalignment				
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	Top-bottom misalignment	Left-right misalignment	Front-rear misalignment															
																		

No.	Process	Condition						
8	Handling after chip mounted  Caution	<p data-bbox="491 219 1490 360">3) When functional check of the P.C.board is performed, check pin pressure tends to be adjusted higher for fear of loose contact. But if the pressure is excessive and bend the P.C.board, it may crack the chip capacitor or peel the terminations off. Please adjust the check pins not to bend the P.C.board.</p> <table border="1" data-bbox="485 383 1484 790"> <thead> <tr> <th data-bbox="485 383 643 450">Item</th> <th data-bbox="643 383 1062 450">Not recommended</th> <th data-bbox="1062 383 1484 450">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="485 450 643 790">Board bending</td> <td data-bbox="643 450 1062 790">  </td> <td data-bbox="1062 450 1484 790">  </td> </tr> </tbody> </table>	Item	Not recommended	Recommended	Board bending		
Item	Not recommended	Recommended						
Board bending								
9	Handling of loose chip capacitor	<p data-bbox="491 833 1490 936">1) If dropped the chip capacitor may crack. Once dropped do not use it. Especially, the large case sized chip capacitor is tendency to have cracks easily, so please handle with care.</p>  <p data-bbox="491 1234 1490 1301">2) Piling the P.C.board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitor of another board to cause crack.</p> 						
10	Estimated life and estimated failure rate of capacitors	<p data-bbox="483 1673 1453 1872">As per the estimated life and the estimated failure rate depend on the temperature and the voltage. This can be calculated by the equation described in JEITA RCR-2335C Annex F (Informative) Calculation of the estimated lifetime and the estimated failure rate (Voltage acceleration coefficient : 3 multiplication rule, Temperature acceleration coefficient : 10°C rule) The failure rate can be decreased by reducing the temperature and the voltage but they will not be guaranteed.</p>						

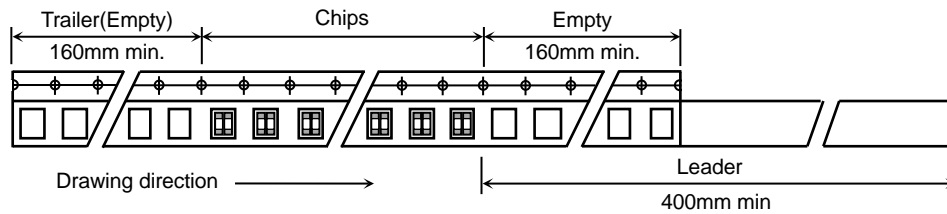
No.	Process	Condition
11	Caution during operation of equipment	<p>1) A capacitor shall not be touched directly with bare hands during operation in order to avoid electric shock. Electric energy held by the capacitor may be discharged through the human body when touched with a bare hand. Even when the equipment is off, a capacitor may stay charged. The capacitor should be handled after being completely discharged using a resistor.</p> <p>2) The terminals of a capacitor shall not be short-circuited by any accidental contact with a conductive object. A capacitor shall not be exposed to a conductive liquid such as an acid or alkali solution. A conductive object or liquid, such as acid and alkali, between the terminals may lead to the breakdown of a capacitor due to short circuit</p> <p>3) Confirm that the environment to which the equipment will be exposed during transportation and operation meets the specified conditions. Do not to use the equipment in the following environments.</p> <p>(1) Environment where a capacitor is splattered with water or oil (2) Environment where a capacitor is exposed to direct sunlight (3) Environment where a capacitor is exposed to Ozone, ultraviolet rays or radiation (4) Environment where a capacitor exposed to corrosive gas(e.g. hydrogen sulfide, sulfur dioxide, chlorine. ammonia gas etc.) (5) Environment where a capacitor exposed to vibration or mechanical shock exceeding the specified limits. (6) Atmosphere change with causes condensation</p>
12	Others  Caution	<p>The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.</p> <p>The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet. If you intend to use the products in the applications listed below or if you have special requirements exceeding the range or conditions set forth in this specification, please contact us.</p> <p>(1) Aerospace/Aviation equipment (2) Transportation equipment (cars, electric trains, ships, etc.) (3) Medical equipment (Excepting Pharmaceutical Affairs Law classification Class1, 2) (4) Power-generation control equipment (5) Atomic energy-related equipment (6) Seabed equipment (7) Transportation control equipment (8) Public information-processing equipment (9) Military equipment (10) Electric heating apparatus, burning equipment (11) Disaster prevention/crime prevention equipment (12) Safety equipment (13) Other applications that are not considered general-purpose applications</p> <p>When designing your equipment even for general-purpose applications, you are kindly requested to take into consideration securing protection circuit/device or providing backup circuits in your equipment.</p>

11. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

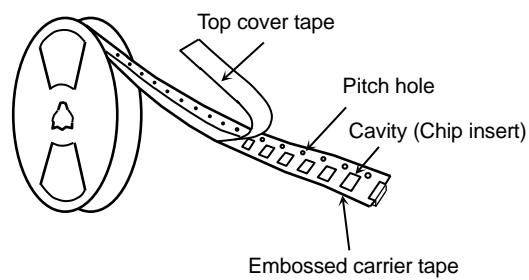
1-1. Dimensions of carrier tape
According to Appendix 3.

1-2. Bulk part and leader of taping



1-3. Dimensions of reel
According to Appendix 4.

1-4. Structure of taping



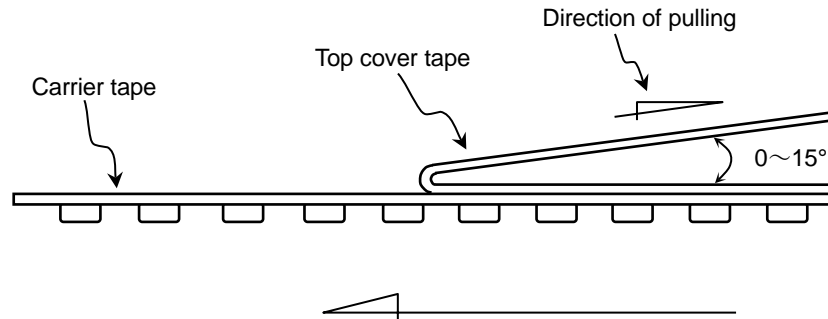
2. CHIP QUANTITY

Please refer to detail page on TDK web.

3. PERFORMANCE SPECIFICATIONS

3-1. Fixing peeling strength (top cover tape)

$$0.05\text{N} < \text{Peeling strength} < 0.7\text{N}$$



3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

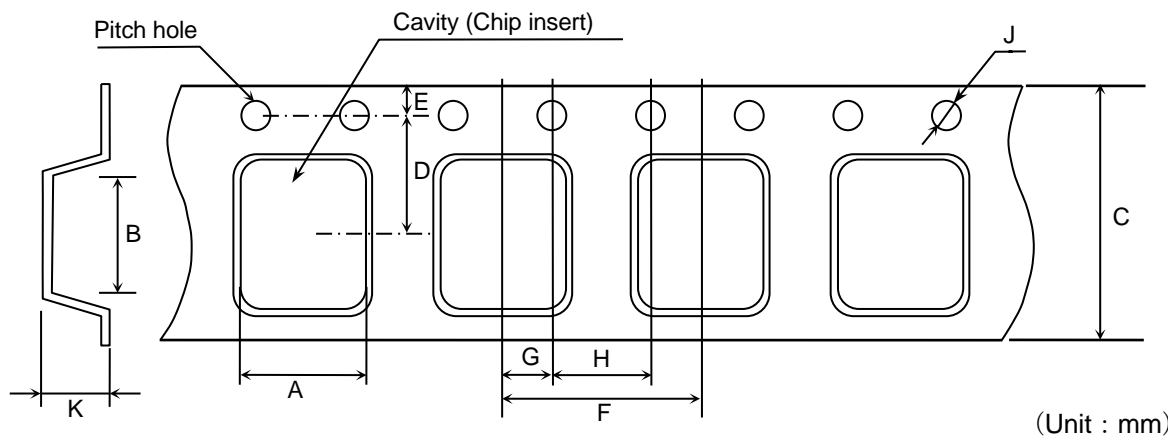
3-3. The missing of components shall be less than 0.1%

3-4. Components shall not stick to fixing tape.

3-5. When removing the cover tape, there shall not be difficulties by unfitting clearance gap, burrs and crushes of cavities. Also the sprocket holes shall not be covered by absorbing dust into the suction nozzle.

Appendix 3

Plastic Tape



(Unit : mm)

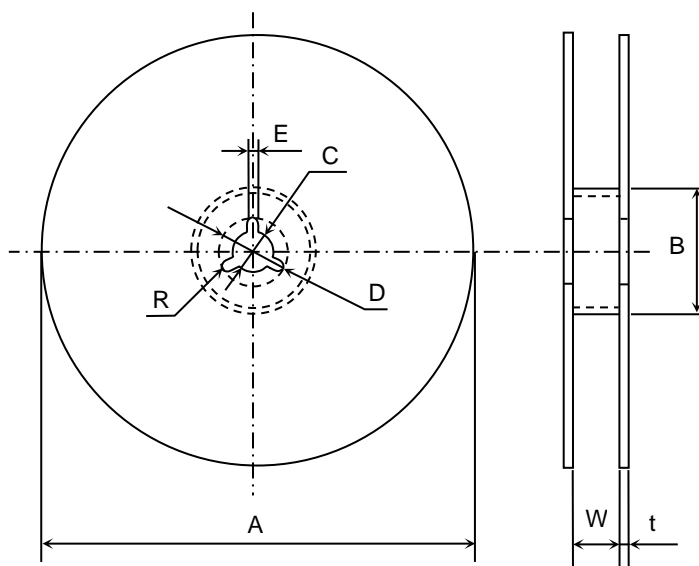
Symbol	A	B	C	D	E	F
CAA572	(5.90)	(6.40)	16.0±0.30	7.50±0.10	1.75±0.10	12.00±0.10
CAA573	(6.40)	(8.70)				

Symbol	G	H	J	K
CAA572	2.00±0.10	4.00±0.10	ø1.50 ^{+0.1} ₀	6.80 max.
CAA573				

() Referenced value.

Appendix 4

(Material : Polystyrene)



(Unit : mm)

Symbol	A	B	C	D	E	W
Dimension	ø382 max. (Nominalø330)	ø50 min.	ø13±0.5	ø21±0.8	2.0±0.5	17.5±1.5

Symbol	t	R
Dimension	2.0±0.5	1.0