

Mains Fail Option

The mains fail option is a factory fitted board providing mains or AC fail and converter inhibit/enable signals. A low power 5V-auxillary supply is also present whenever mains supply is connected to the PSU.

The option attaches to either a module or blank chassis occupying the right hand slot 1 position looking at the output modules.

There are five types of mains fail option available: -

(1) Standard mains fail 'MF' option – provides open-collector mains fail signal, active high or low converter inhibit, and 5V auxiliary supply. Mains fail and inhibit signals are referenced to the 5V auxiliary return.

(2) Latching mains fail 'MFL' option – functionally similar to the standard mains fail 'MF' option except the first operation of converter inhibit signal turns the converter off permanently. The outputs can only be re- established by cycling the PSU mains input off (for 20seconds) and then back on.

(3) Mains fail with enable 'MFE' option – functionally similar to the standard mains fail 'MF' operation except that the inhibit signal is replaced with enable signal. The PSU outputs remain off unless and active high or low enable signal is applied.

(4) Mains fail with floating/uncommitted output 'MFU' option – functionally similar to the standard mains fail 'MF' option except the mains fail signal has a floating or uncommitted transistor output enabling active high or low mains fail signals to be realised depending on the application circuit.

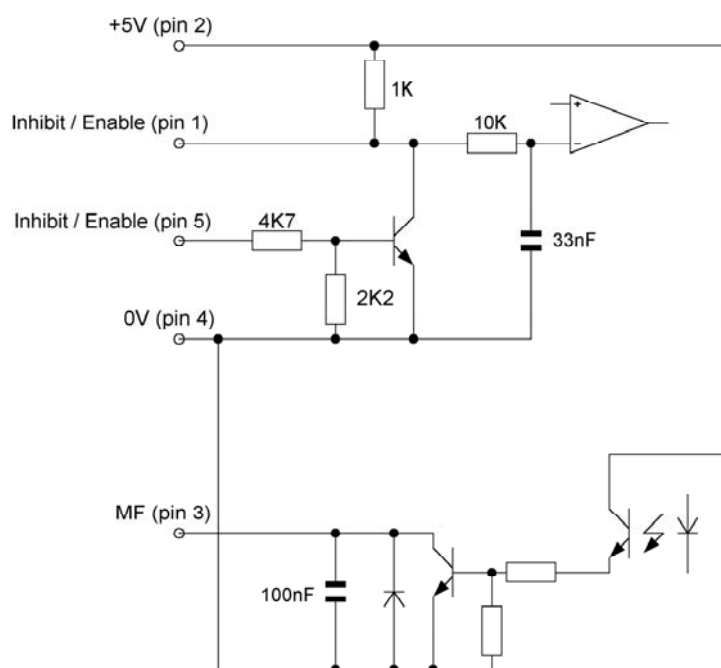
(5) The Power monitor 'MFV' option for the VMEbus and VXIbus is used to generate the signals ACFAIL and SYSRESET. Monitoring the supply and output, a controlled shutdown of the system will be performed in the event of an AC power failure or a change in the 5V-output, of +5% or -2.5%. When the system is powered up or down a controlled signal sequence is initialised. The timing sequence of the generated signals ACFAIL and SYSRESET can be found in detail in the VMEbus specification and timing diagrams section.

Standard Mains Fail 'MF' and Latching Mains Fail 'MFL' option

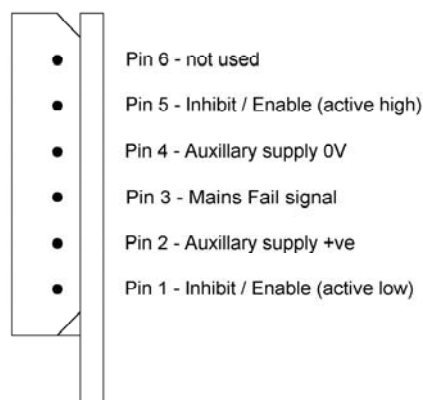
Specifications - all voltages with respect to auxiliary 0Volts (pin 4) unless otherwise stated

Active low Inhibit – pin 1	
Max Inhibit voltage for PSU off	0.8V max (sink current typically 5mA)
Min Inhibit voltage for PSU on	2.0V min
Open circuit Inhibit voltage	5V
Delay time Inhibit to outputs off	typ 0.65mS (see timing diagrams)
Delay time Inhibit to outputs on	CA400,CA1000 typ 0.2mS ; CA600 typ 0.43mS
PSU i/p power when Inhibited	CA400 typ 12W, CA600 typ 15W, CA1000/1250 typ 26W
Active high Inhibit – pin 5	
Min Inhibit voltage for PSU off	2.0V min
Max Inhibit voltage for PSU on	0.8V max
Source current Inhibit = 5V	typ 1mA
Source current Inhibit = 12V	typ 2.5mA
Max Inhibit voltage	15V max
Mains Fail signal – pin 3	
Max sink current	50mA max
Max open circuit voltage	50V max
Warning time to DC output fall	5mS min (see timing diagrams)
Auxiliary supply – pin 2 to pin 4	
Output voltage	5V +/- 5% (+ve pin 2, -ve pin 4)
Max continuous output current	50mA max
Overload protection	thermal shutdown
Auxiliary output rise	typ >50mS before DC outputs rise (see timing diagrams)
Auxiliary output fall	typ >1.5S after DC outputs fall (see timing diagrams)
Isolation to earth	500V DC max

Internal Schematic



Connection Details



Mating Connector Details (parts supplied)

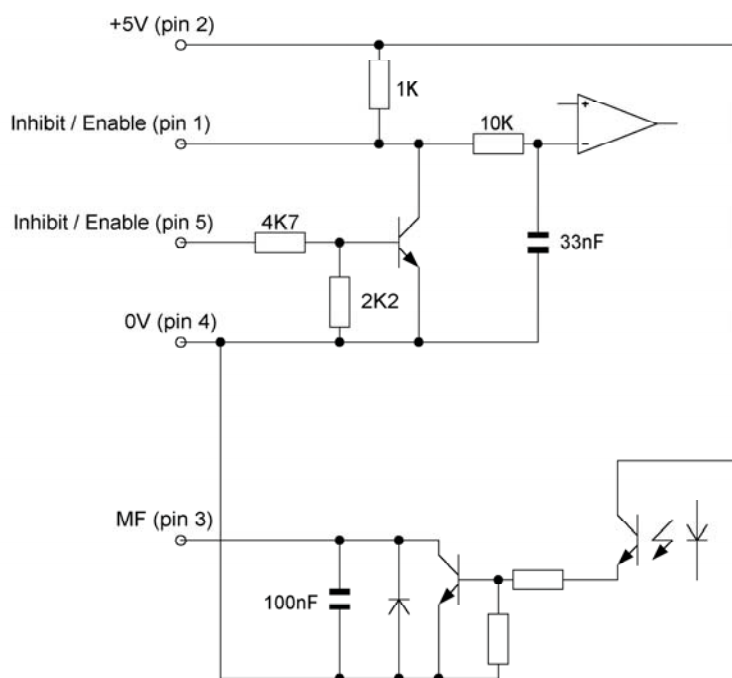
6-way housing : Molex 5264-N series
Molex Part No. 50-37-5063
Crimp terminals : Molex 5263 series
Molex Part No. 08-70-1039 (chain)

Mains Fail with converter enable 'MFE' option

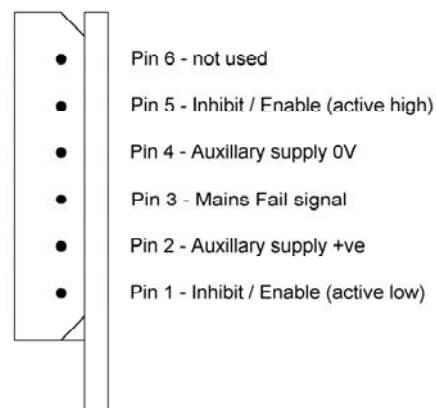
Specifications - all voltages with respect to auxiliary 0Volts (pin 4) unless otherwise stated

Active low enable – pin 1	
Max enable voltage for PSU on	0.8V max (sink current typically 5mA)
Min enable voltage for PSU off	2.0V min
Open circuit enable voltage	5V
Delay time enable to outputs off	typ 0.65mS (see timing diagrams)
Delay time enable to outputs on	CA400, CA1000 typ 0.2mS ; CA600 typ 0.43mS
PSU i/p power when not enabled	CA400 typ 12W, CA600 typ 15W, CA1000/1250 typ 26W
Active high enable – pin 5	
Min enable voltage for PSU on	2.0V min
Max enable voltage for PSU off	0.8V max
Source current enable = 5V	typ 1mA
Source current enable = 12V	typ 2.5mA
Max enable voltage	15V max
Mains Fail signal – pin 3	
Max sink current	50mA max
Max open circuit voltage	50V max
Warning time to DC output fall	5mS min (see timing diagrams)
Auxiliary supply – pin 2 to pin 4	
Output voltage	5V +/- 5% (+ve pin 2, -ve pin 4)
Max continuous output current	50mA max
Overload protection	thermal shutdown
Auxiliary output rise	typ >50mS before DC outputs rise (see timing diagrams)
Auxiliary output fall	typ >1.5S after DC outputs fall (see timing diagrams)
Isolation to earth	500V DC max

Internal Schematic



Connection Details



Mating Connector Details (parts supplied)

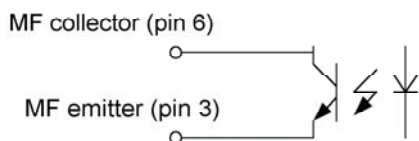
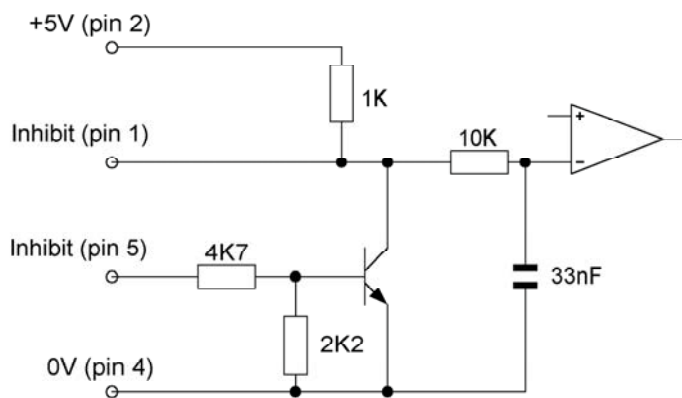
6-way housing : Molex 5264-N series
Molex Part No. 50-37-5063
Crimp terminals : Molex 5283 series
Molex Part No. 08-70-1039 (chain)

Mains Fail with floating/uncommitted output signal 'MFU' option

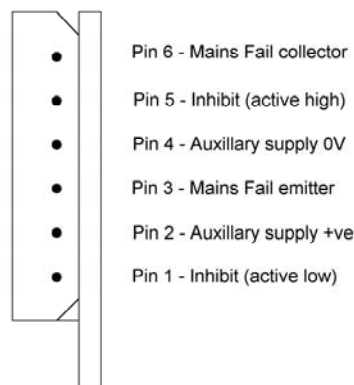
Specifications - all voltages with respect to auxiliary 0Volts (pin 4) unless otherwise stated

Active low Inhibit – pin 1	
Max Inhibit voltage for PSU off	0.8V max (sink current typically 5mA)
Min Inhibit voltage for PSU on	2.0V min
Open circuit Inhibit voltage	5V
Delay time Inhibit to outputs off	typ 0.65mS (see timing diagrams)
Delay time Inhibit to outputs on	CA400,CA1000 typ 0.2mS ; CA600 typ 0.43mS
PSU i/p power when Inhibited	CA400 typ 12W, CA600 typ 15W, CA1000/1250 typ 26W
Active high Inhibit – pin 5	
Min Inhibit voltage for PSU off	2.0V min
Max Inhibit voltage for PSU on	0.8V max
Source current Inhibit = 5V	typ 1mA
Source current Inhibit = 12V	typ 2.5mA
Max Inhibit voltage	15V max
Mains Fail signal – pin 3 & pin 6	
Optocoupler transistor collector	connector pin 6
Optocoupler transistor emitter	connector pin 3
Max collector current for $V_{ce} < 0.8V$	5mA max
Max collector-emitter voltage	50V max
Warning time to DC output fall	5mS min (see timing diagrams)
Max float voltage with respect to pin4	50V max
Auxiliary supply – pin 2 to pin 4	
Output voltage	5V +/- 5% (+ve pin 2, -ve pin 4)
Max continuous output current	50mA max
Overload protection	thermal shutdown
Auxiliary output rise	typ >50mS before DC outputs rise (see timing diagrams)
Auxiliary output fall	typ >1.5S after DC outputs fall (see timing diagrams)
Isolation to earth	500V DC max

Internal Schematic



Connection Details



Mating Connector Details (parts supplied)

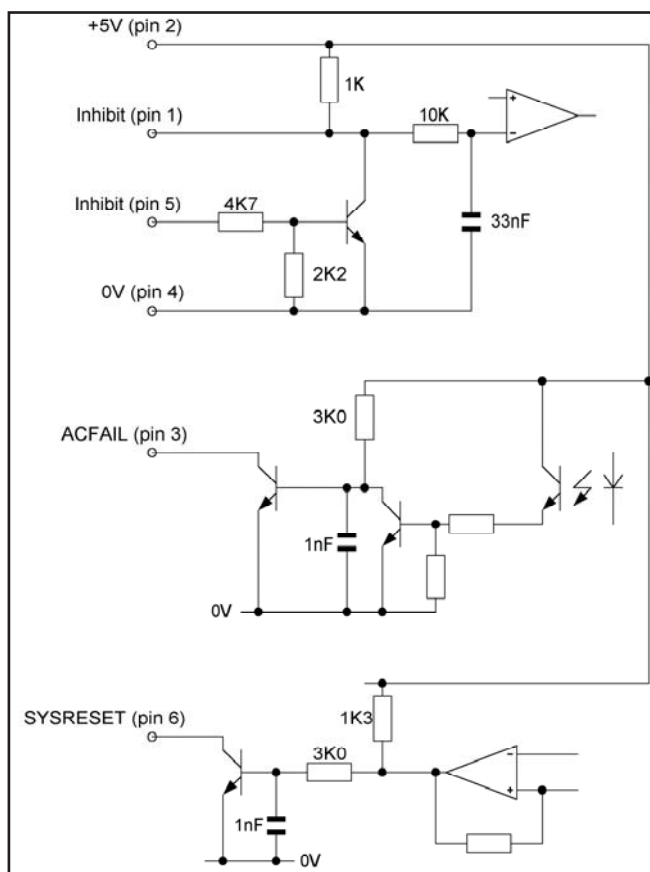
6-way housing : Molex 5264-N series
Molex Part No. 50-37-5063
Crimp terminals : Molex 5263 series
Molex Part No. 08-70-1039 (chain)

Power Monitor 'MFV' option for the VMEbus and VXibus

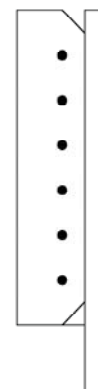
Specifications - all voltages with respect to auxiliary 0Volts (pin 4) unless otherwise stated

Active low Inhibit – pin 1	
Max Inhibit voltage for PSU off	0.8V max (sink current typically 5mA)
Min Inhibit voltage for PSU on	2.0V min
Open circuit Inhibit voltage	5V
Delay time Inhibit to outputs off	typ 0.65mS (see timing diagrams)
Delay time Inhibit to outputs on	CA400,CA1000 typ 0.2mS ; CA600 typ 0.43mS
PSU i/p power when Inhibited	CA400 typ 12W, CA600 typ 15W, CA1000/1250 typ 26W
Active high Inhibit – pin 5	
Min Inhibit voltage for PSU off	2.0V min
Max Inhibit voltage for PSU on	0.8V max
Source current Inhibit = 5V	typ 1mA
Source current Inhibit = 12V	typ 2.5mA
Max Inhibit voltage	15V max
Auxiliary supply – pin 2 to pin 4	
Output voltage	5V +/- 5% (+ve pin 2, -ve pin 4)
Max continuous output current	50mA max
Overload protection	thermal shutdown
Auxiliary output rise	typ >50mS before DC outputs rise (see timing diagrams)
Auxiliary output fall	typ >1.5S after DC outputs fall (see timing diagrams)
Isolation to earth	500V DC max
ACFAIL – pin 3	
Max sink current	100mA max for ACFAIL<0.8V
Max open circuit voltage	38V max
Warning time	5ms min (see timing diagrams and VME specification)
SYSRESET – pin 6	
Max sink current	100mA max for SYSRESET<0.8V
Max open circuit voltage	38V max
Controlled operating time	see timing diagrams and VMEbus specification

Internal Schematic



Connection Details



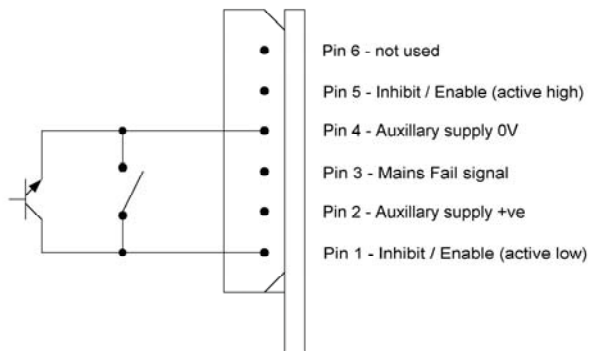
- Pin 6 - SYSRESET (active low)
- Pin 5 - Inhibit (active high)
- Pin 4 - Auxillary supply 0V
- Pin 3 - ACFAIL (active low)
- Pin 2 - Auxillary supply +ve
- Pin 1 - Inhibit (active low)

Mating Connector Details
(parts supplied)

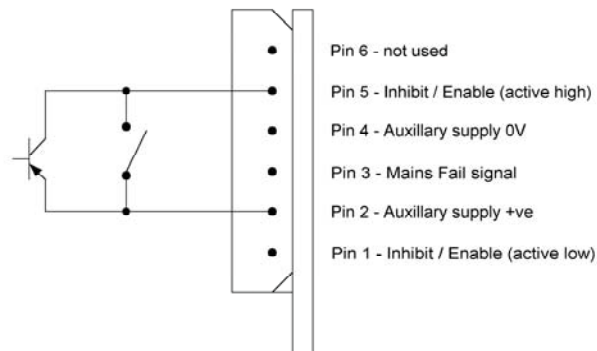
- 6-way housing : Molex 5264-N series
Molex Part No. 50-37-5063
- Crimps terminals : Molex 5263 series
Molex Part No. 08-70-1039 (chain)

Typical Application Circuits

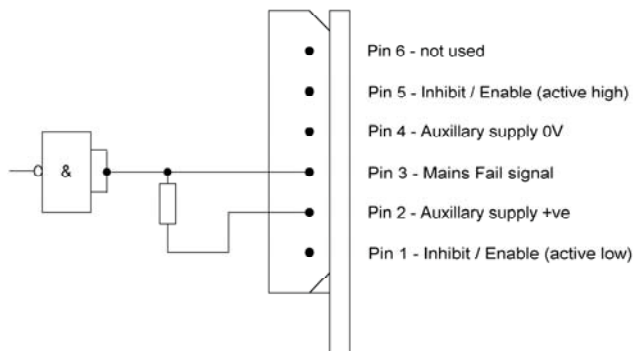
Active low inhibit/enable with switch / relay contact or open collector transistor



Active high inhibit/enable with switch / relay contact or open collector transistor

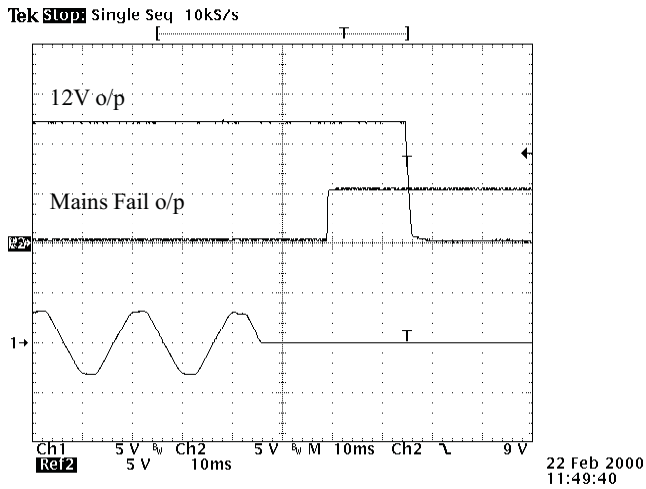


Mains Fail Warning (MF, MFL, MFE options)



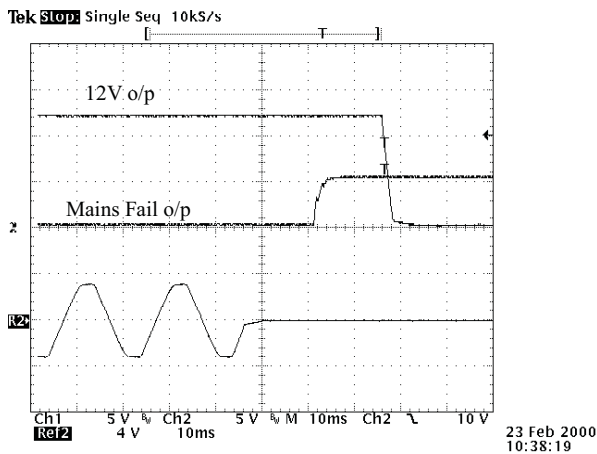
Typical Timing Diagrams – Mains Fail Signal

Alpha 400 typical timing at switch-off (230V, 400W, ambient=25DegC)



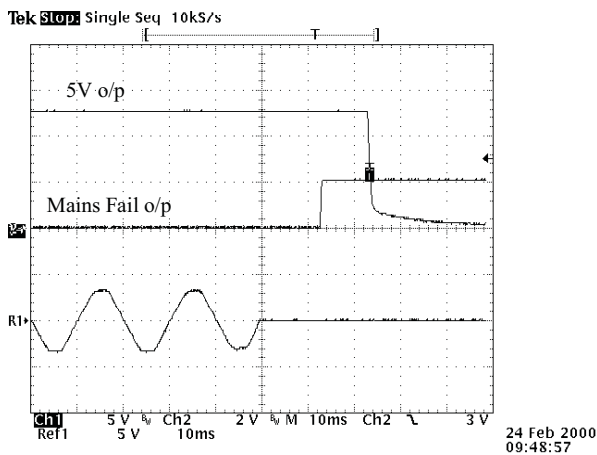
10mS per division
Typical initial hold-up = 29mS
Typical initial warning time = 15mS

Alpha 600 typical timing at switch-off (230V, 600W, ambient=25DegC)

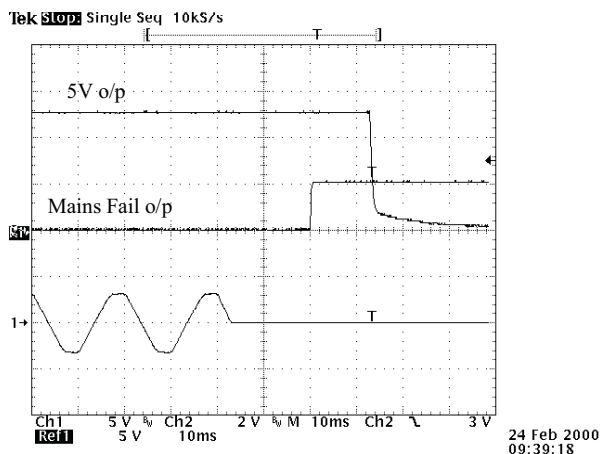


10mS per division
Typical initial hold-up = 30mS
Typical initial warning time = 11mS

Alpha1000 timing at switch-off (230V,1000W)
 (10mS per division)
 (Typical initial hold-up=23mS)
 (Typical initial warning=19mS)

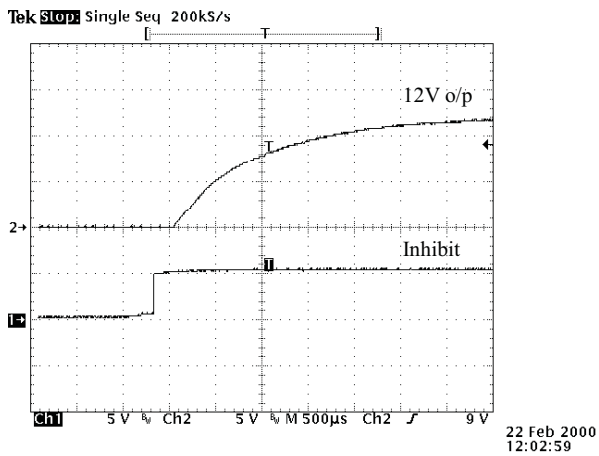


Alpha1000 timing at switch-off (230V,800W)
 (10mS per division)
 (Typical initial hold-up=30mS)
 (Typical initial warning=12mS)

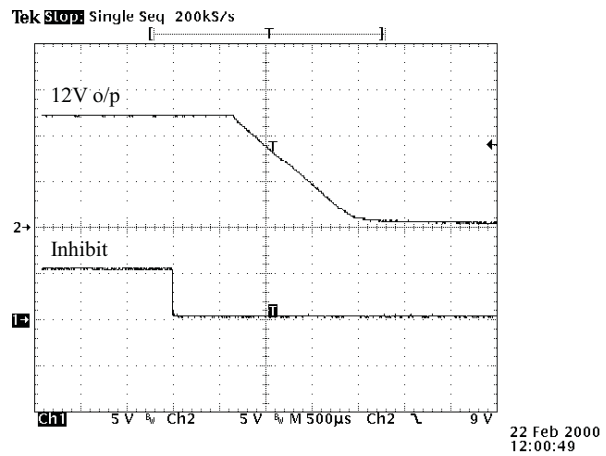


Typical Timing Diagrams – Converter Inhibit

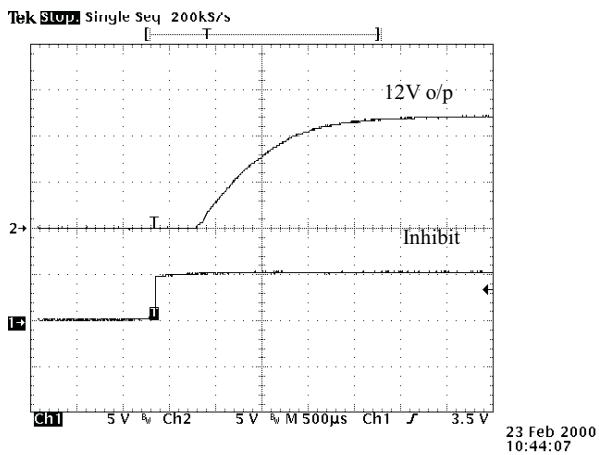
CA400 Converter Inhibit to output rise delay
(500uS per division, delay typically 220uS)



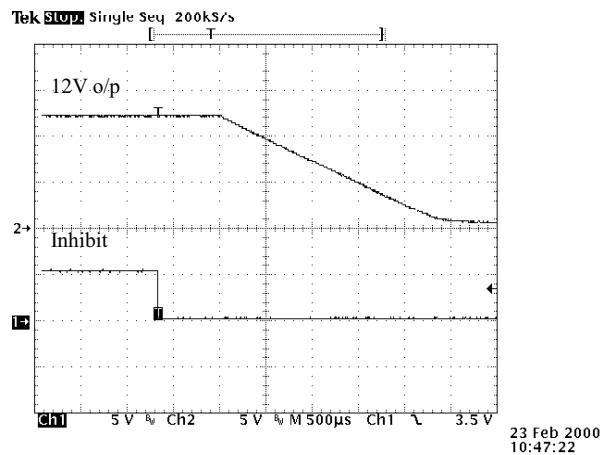
CA400 Converter Inhibit to output fall delay
(500uS per division, delay typically 650uS)



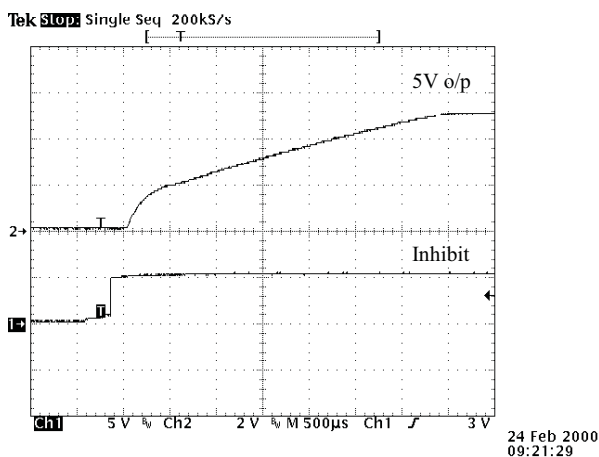
CA600 Converter Inhibit to output rise delay
(500uS per division, delay typically 430uS)



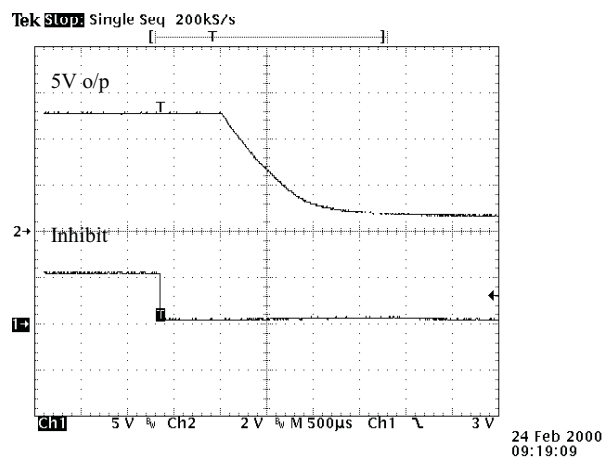
CA600 Converter Inhibit to output fall delay
(500uS per division, delay typically 660uS)



CA1000 Converter Inhibit-output rise delay
(500uS per division, delay typically 180uS)

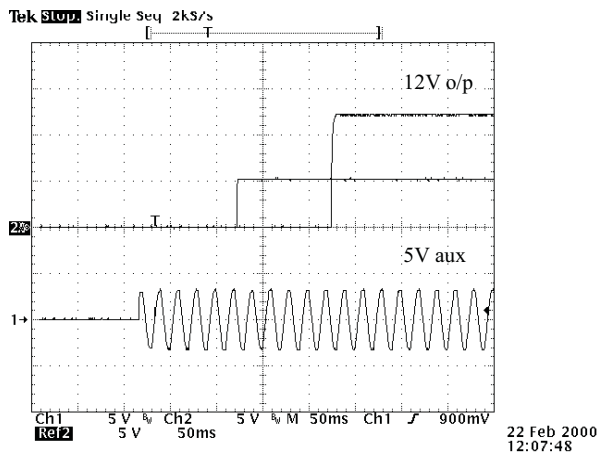


CA1000 Converter Inhibit-output fall delay
(500uS per division, delay typically 650uS)

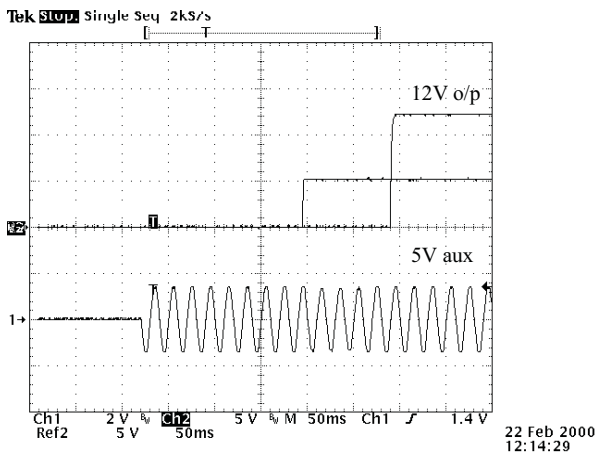


Typical Timing Diagrams – Alpha 400 Auxillary Supply

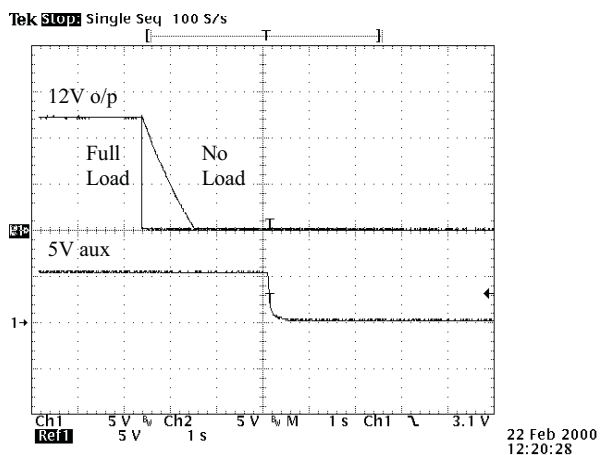
CA400 5V auxiliary & output rise (230Vac)
(50mS per div, 5V aux delay typ 107mS)



CA400 5V auxiliary & output rise (100Vac)
(50mS per div, 5V aux delay typ 180mS)

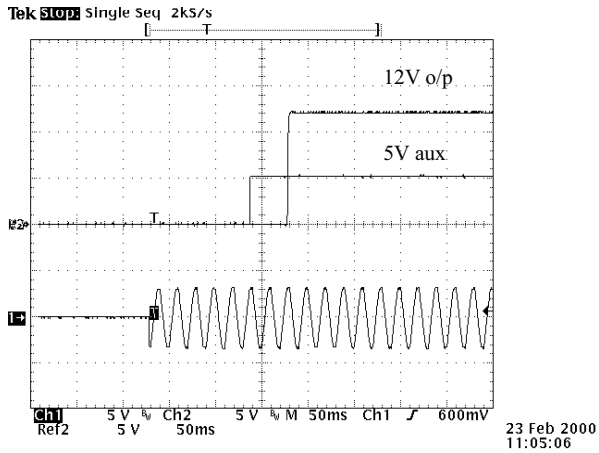


CA400 5V auxiliary & output fall (230Vac)
(1Sec per div, 5V aux delay typ 2.75Sec)

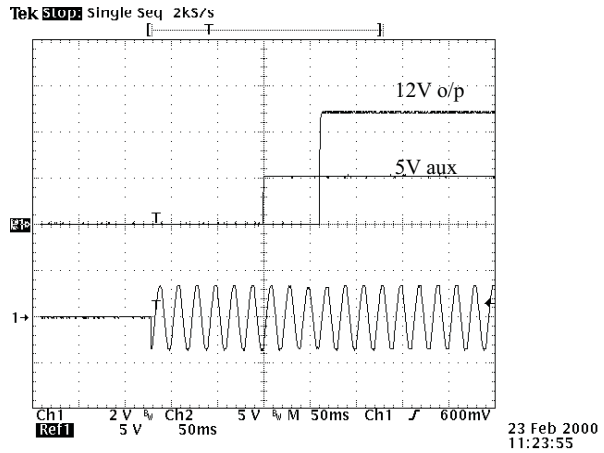


Typical Timing Diagrams – Alpha 600 Auxillary Supply

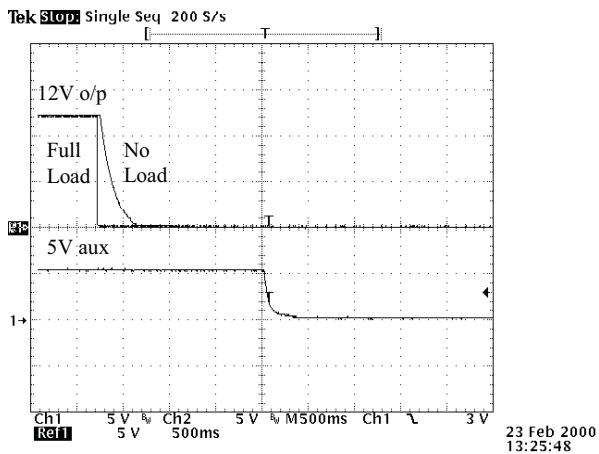
CA600 5V auxiliary & output rise (230Vac)
(50mS per div, 5V aux delay typ 110mS)



CA600 5V auxiliary & output rise (100Vac)
(50mS per div, 5V aux delay typ 120mS)

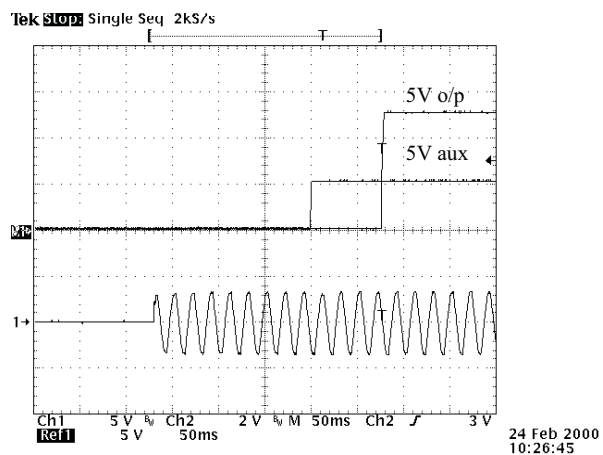


CA600 5V auxiliary & output fall (230Vac)
(1Sec per div, 5V aux delay typ 1.8Sec)

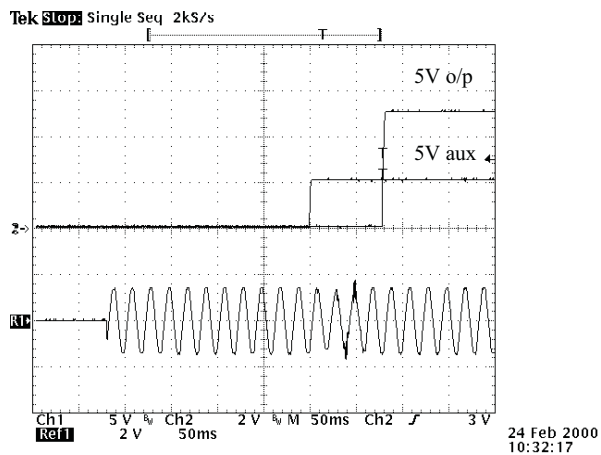


Typical Timing Diagrams – Alpha 1000/1250 Auxillary Supply

CA1000 5V auxiliary & output rise (230Vac)
(50mS per division)
(5V auxiliary delay typically 170mS)

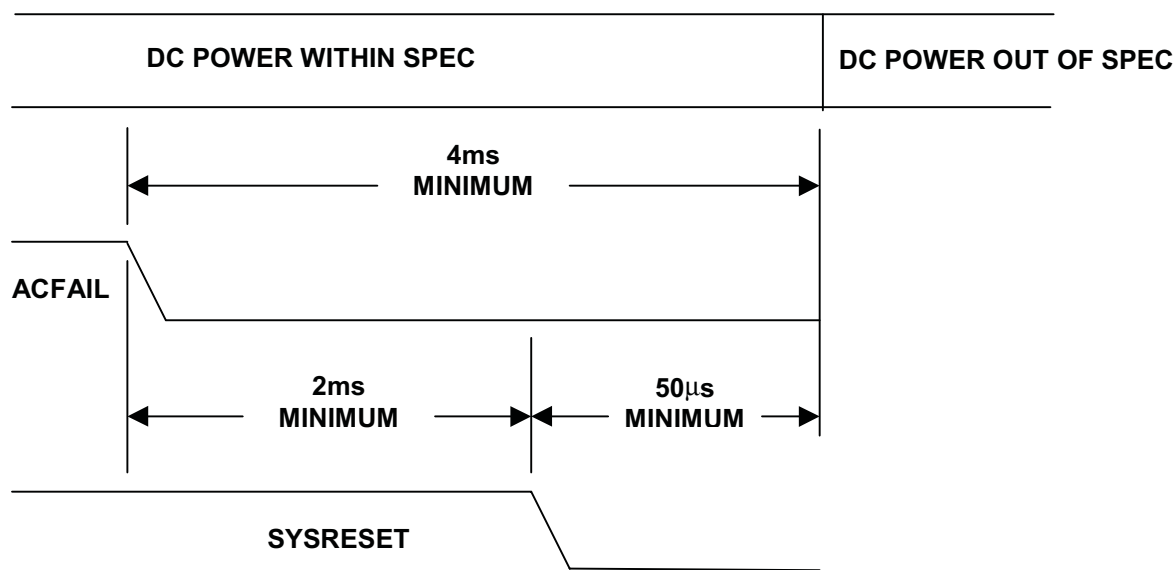


CA1000 5V auxiliary & output rise (100Vac)
(50mS per division)
(5V auxiliary delay typically 220mS)

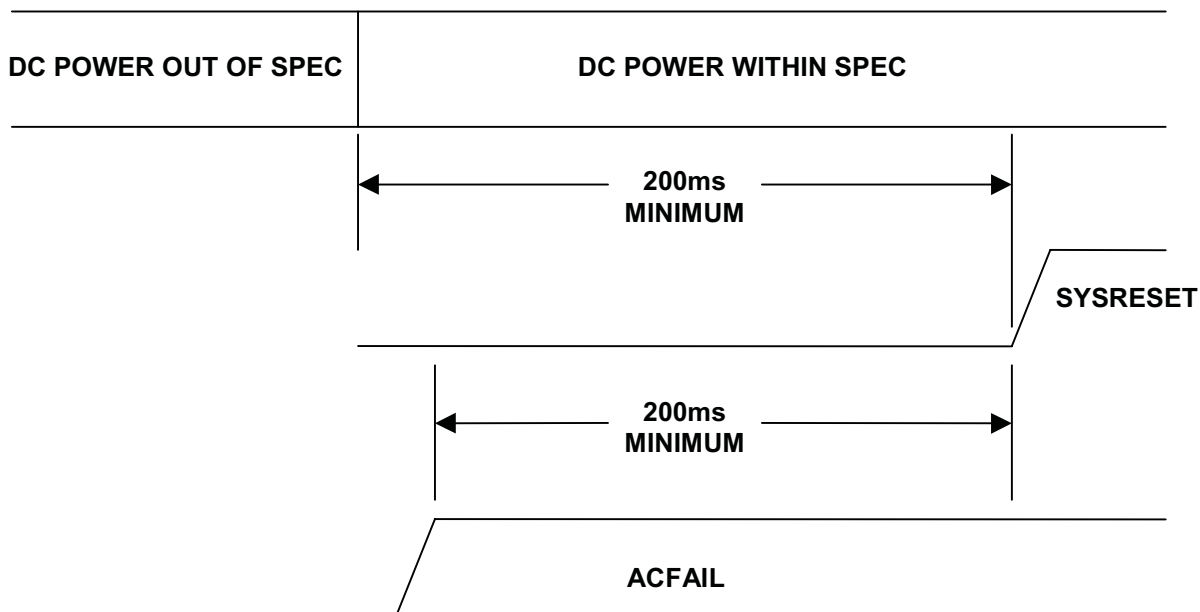


Typical Timing Diagrams – Controlled ACFAIL & SYSRESET Signals

VMEbus SPECIFICATION.



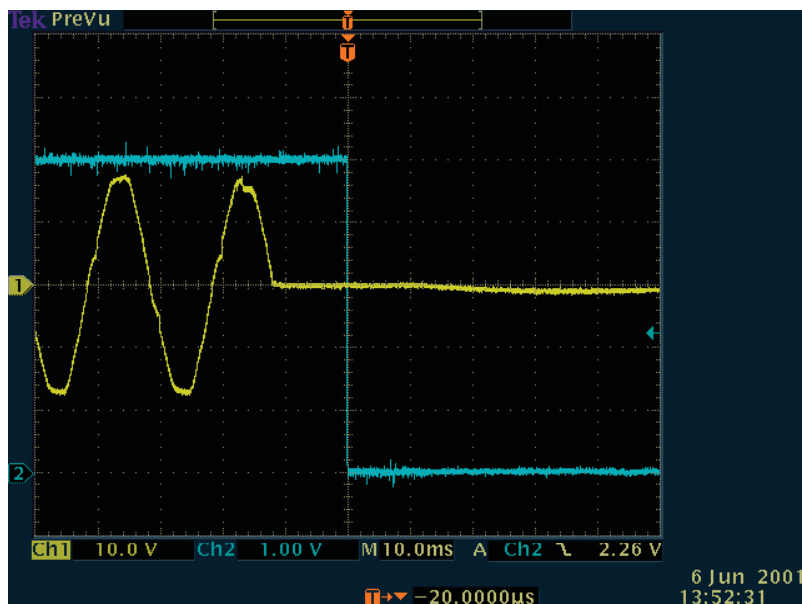
POWER DOWN.
System power fail timing



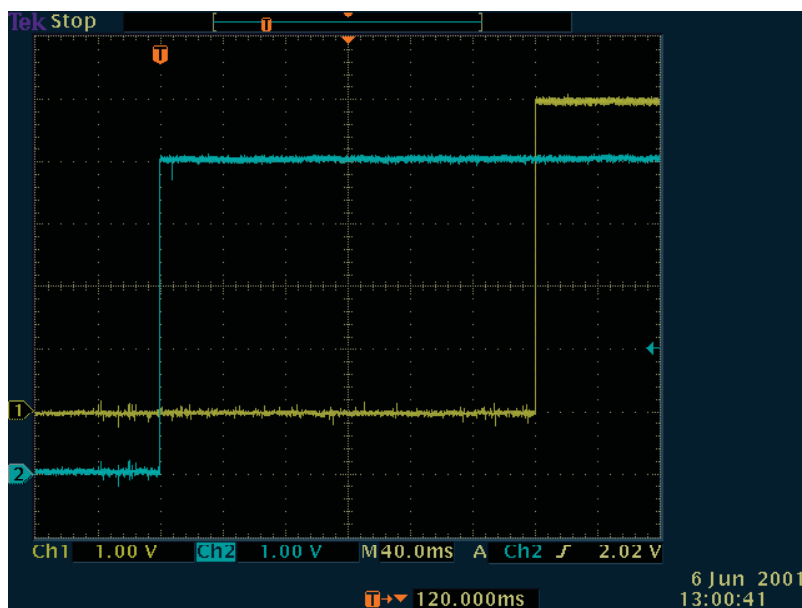
POWER UP.
System power restart timing.

Typical Timing Diagrams – Controlled ACFAIL & SYSRESET Signals

Alpha 400 typical timing at Power Up and Power Down (230V, 400W, ambient=25°C).
 ACFAIL signal prior to power down » 15ms
 10ms per Division



Controlled SYSRESET on Power Up.
 Chn. 2 ACFAIL, Chn. 1 SYSRESET.
 On Power Up, SYSRESET driven low until AC power and DC power within spec, after which SYSRESET is held low for a period of 200ms minimum.
 Typical duration 240ms.
 40ms per Division



Typical Timing Diagrams – Controlled ACFAIL & SYSRESET Signals

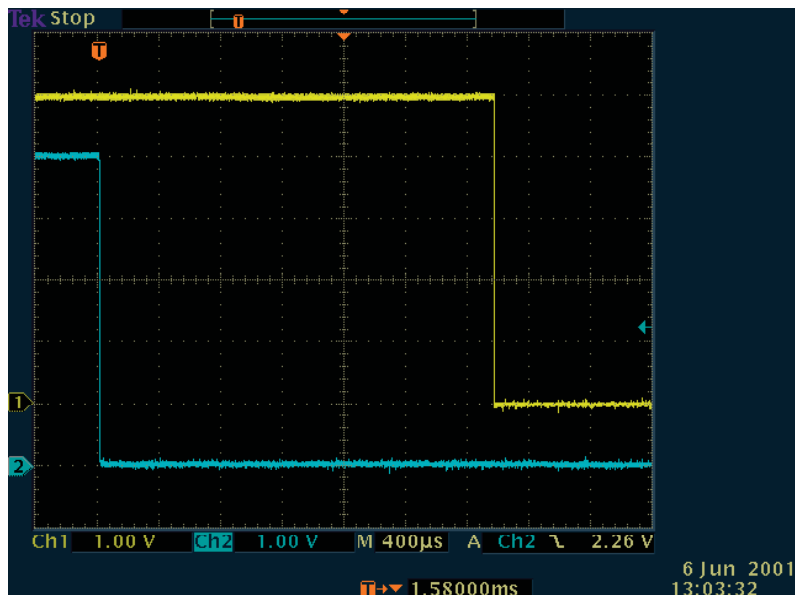
Controlled SYSRESET on Power Down.

Chn. 2 ACFAIL, Chn. 1 SYSRESET.

On Power Down or if the DC O/P voltage falls out of spec the SYSRESET is driven low at a specified interval of 2ms minimum after the event.

Typical Duration 2.5ms.

400ms per Division

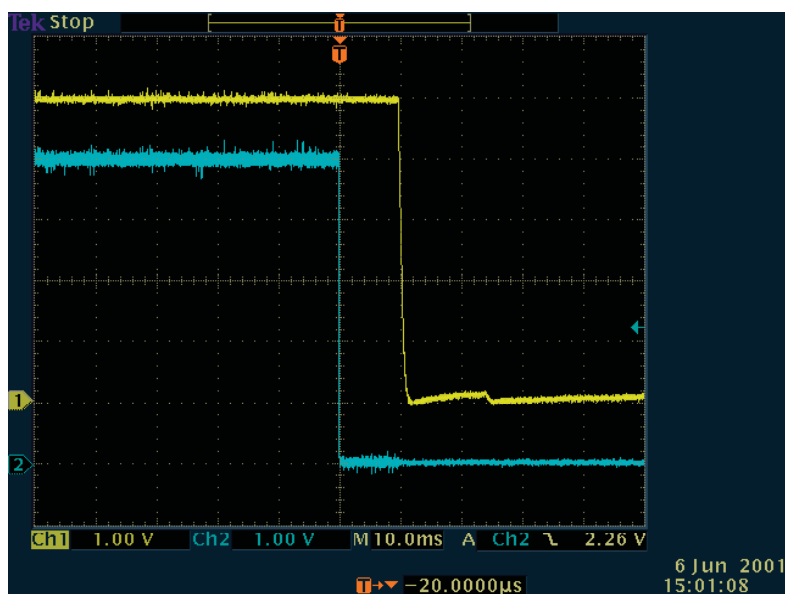


5V O/P after SYSRESET driven low, minimum specified 50ms before 5V O/P falls below spec.

Chn 1 SYSRESET, Chn 2 5V O/P.

Typical 10ms hold up, 400W Alpha.

10ms per Division



VMEbus Application notes

- The Power Monitor 'MFV' option uses the +ve and -ve voltage sense connections to monitor the back plane voltage, due to the inherent voltage drop in the conductors connecting the PSU to the back plane. This implies that the remote sense lines must be connected to the back plane at all times.
- Load swings exceeding 25% can give rise to transients exceeding the power monitor window of +5% and -2.5%. Further decoupling capacitance connected to the back plane can improve transient response overshoot.
- The Alpha customer application manual should be referenced, detailing module specification.
- Paralleling modules using the PP option with the MFV option also requires the connection of the remote sense lines to the back plane at all times via the PP 6-way option molex connector.