



EV1525-0800-100A

EVALUATION BOARD

USER GUIDE

Introduction

This user guide describes the evaluation board provided for the FS1525 μ POL™ product.

The board generates an output voltage (V_{OUT}) of 0.8V* for loads of 0–100A from an input voltage (PV_{IN}) of 12V.

Specifications

- Input voltage (PV_{IN}) = +12V
- Output voltage (V_{OUT}) = +0.8V
- Output load (I_o) = 0–100A
- Switching frequency (F_{SW}) = 625 kHz
- Output capacitance (C_o) = 54x47 μ F (MLCC), 2x470 μ F SP Cap, 1x0.1 μ F (MLCC)
- Input capacitance (C_{IN}) = 2x 68 μ F, 16x22 μ F (MLCC), 4x1 μ F (MLCC)
- Dimensions (width x length x thickness) = 55mm x 14.5mm x 3.8mm

Connections

Name	Identifier	Description
PV_{IN}	J1	Input voltage (+12V)
PGnd	J2	Ground for input voltage
V_{OUT}	J3,J4	Output voltage (+0.8V)
PGnd	J5,J6	Ground for output voltage
V_{IN}	V_{IN}	Test Point for LDO Input
V_{CC}	V_{CC}	Test Point for LDO Output
PGnd	PGnd	Power ground
En	En	Enable
PGood	PGood	Power Good
SCL	SCL	PIN1 I2C/PMBUS clock line
SDA	SDA	PIN2 I2C/PMBUS data line
ALERT	ALERT	SMBALERT#
FAULT	FAULT	FAULT
Load	J7, J8	Used to connect load: 20-pin Intel Mini Slammer connector
Output transient ripple voltage	J10	Used for measurement: 50 Ω ultra-miniature coaxial connector

The board is configured for a single input supply. The Enable (En) input is connected to PV_{IN} through a resistor divider, so that no external Enable signal is needed.

Operation

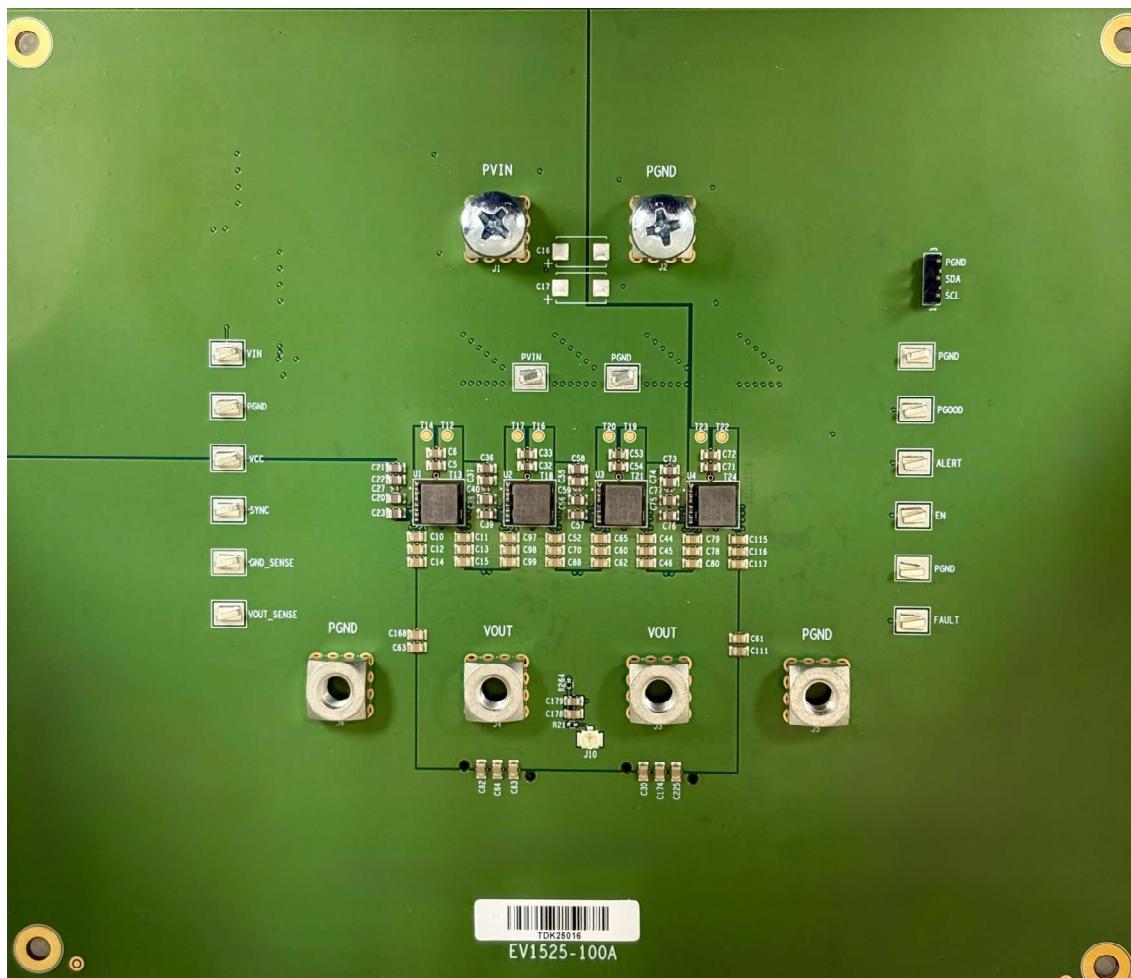
To use the evaluation board:

1. Connect a well-regulated +12V input supply to PV_{IN} (J1) and Gnd (J2).
2. Connect a load of 0–100A to V_{OUT} (J3,J4) and Gnd (J5,J6).

*NOTE – Output Voltages from 0.6V to 1.8V can be obtained by changing the values of Resistor Divider Components. Refer Page 7.

Description

The evaluation board consists of a 8-layer PCB made from FR4 glass-reinforced epoxy laminate material. All layers use 2oz copper. (The major power components, including the FS1525, are mounted on the top side of the board.)



View of board (top)

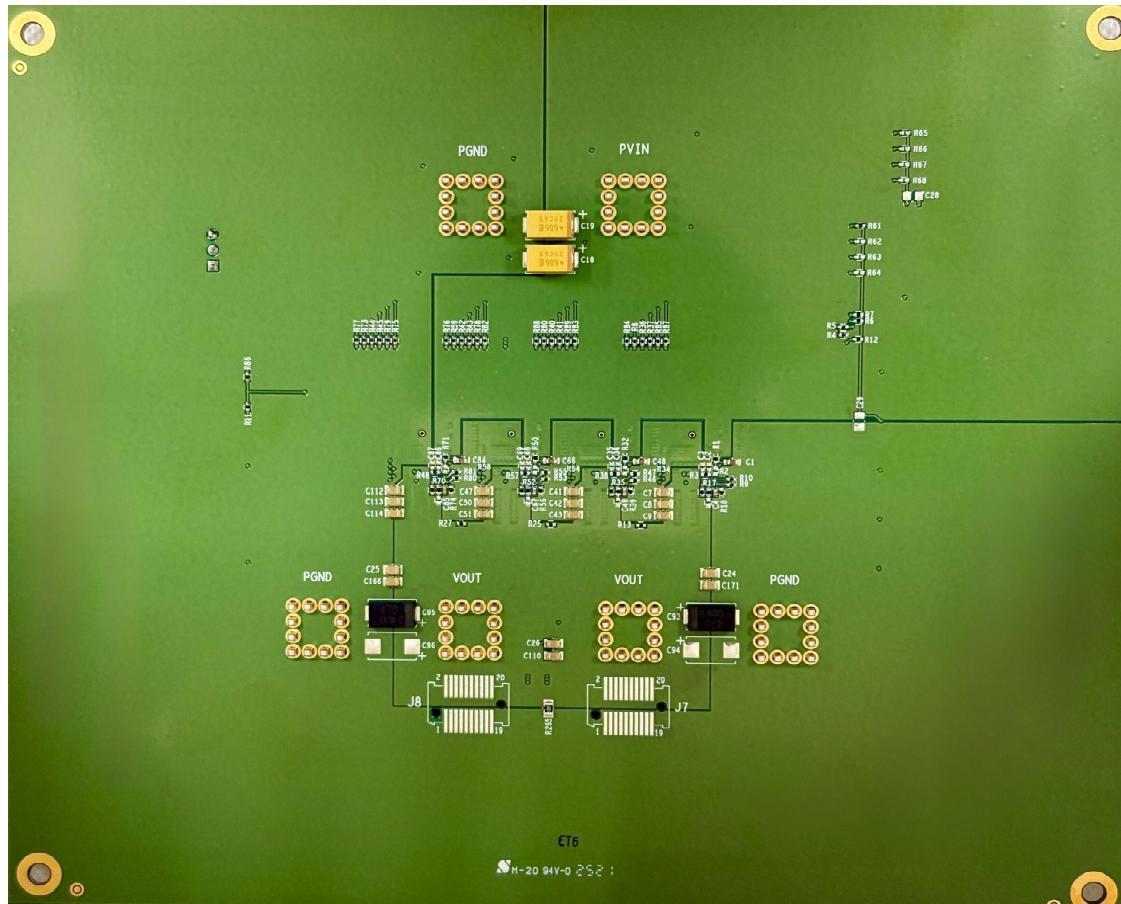


Figure 1 View of board (bottom)

Figure 2 to Figure 11 show the layout of the board layers and Figure 12 shows a schematic of the electric circuit.

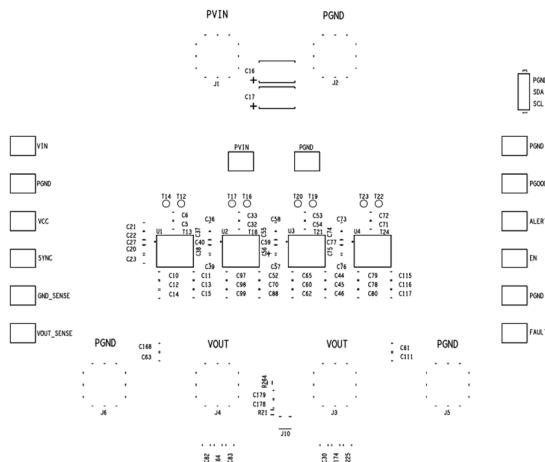


Figure 2 Board layout – SilkScreen Top

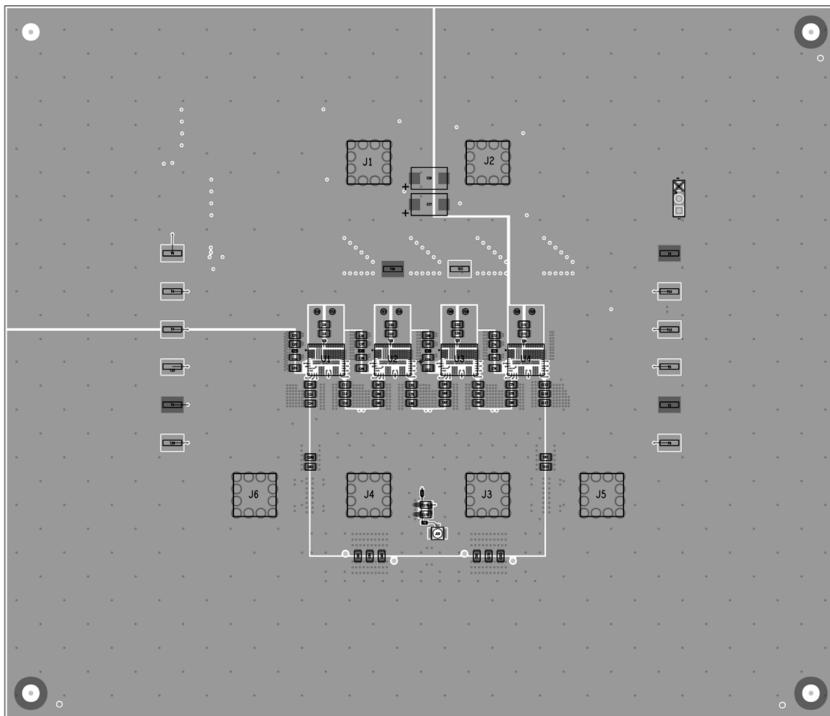


Figure 3 *Board layout – layer 1*

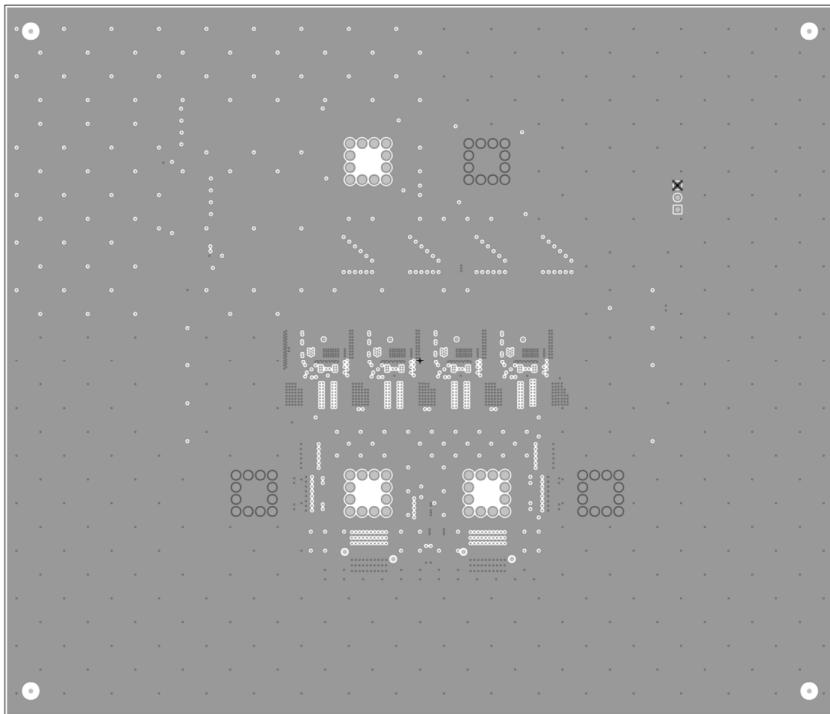


Figure 4 Board layout – layer 2

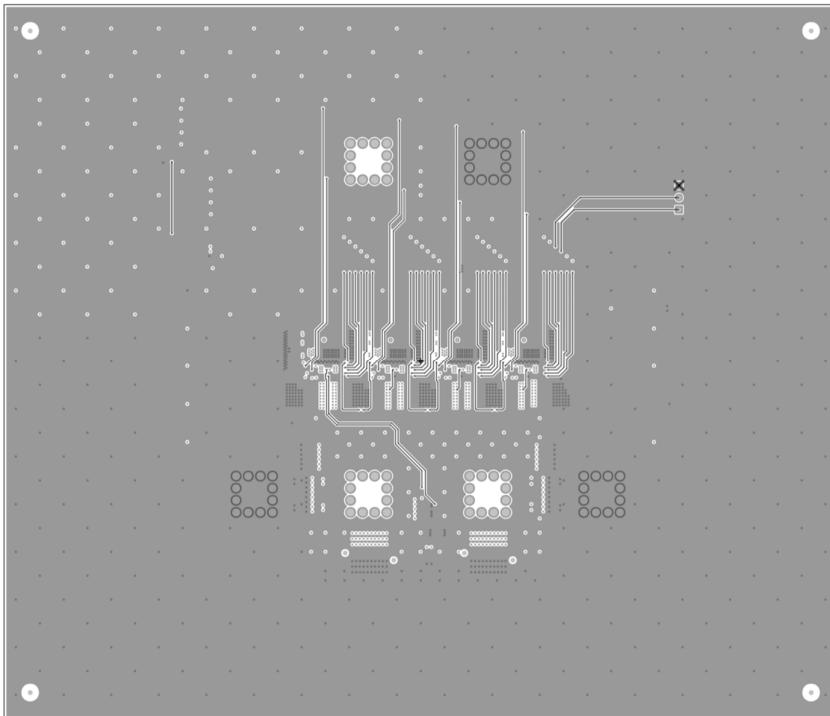


Figure 5 *Board layout – layer 3*

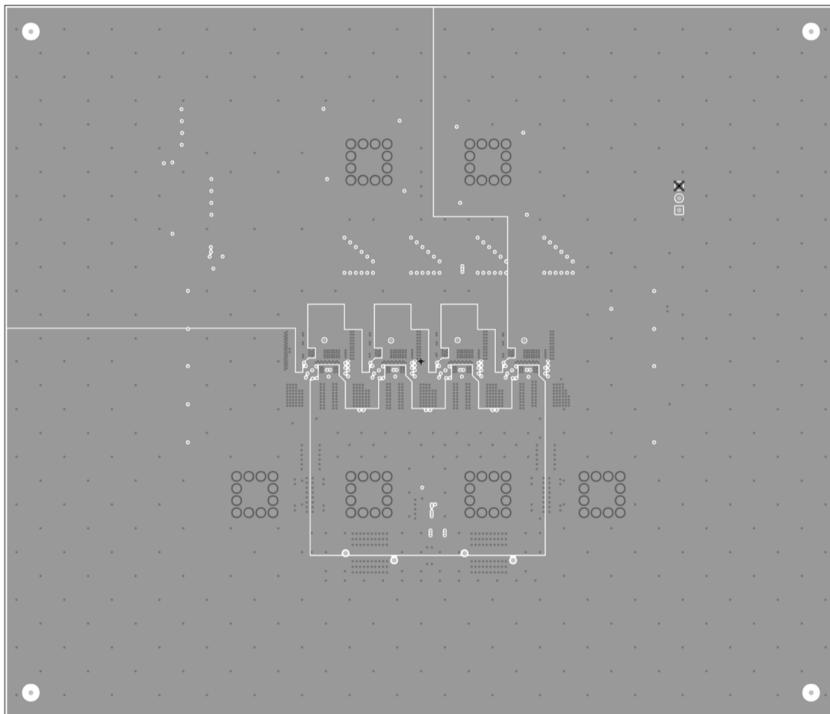


Figure 6 *Board layout – layer 4*

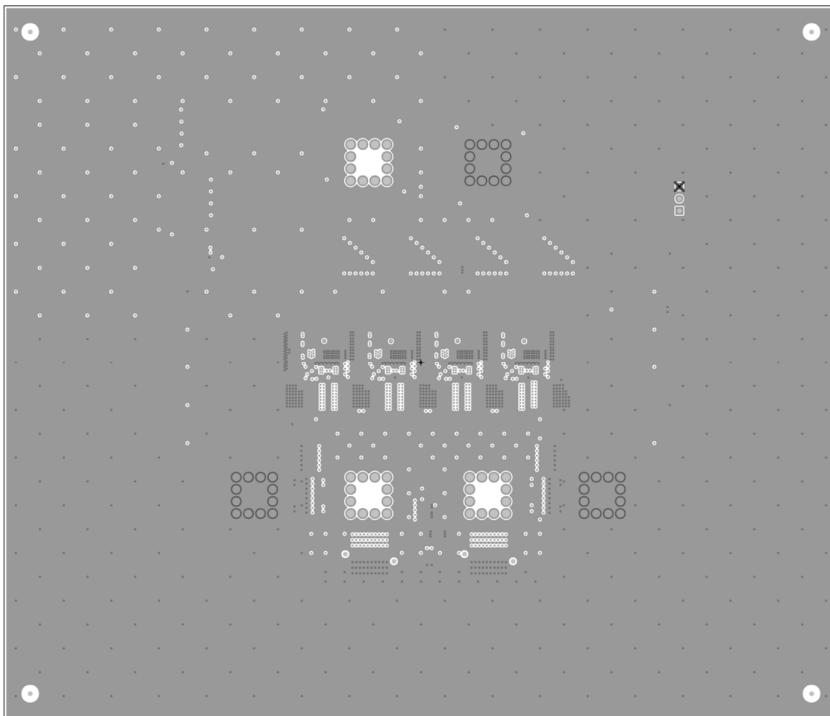


Figure 7 *Board layout – layer 5*

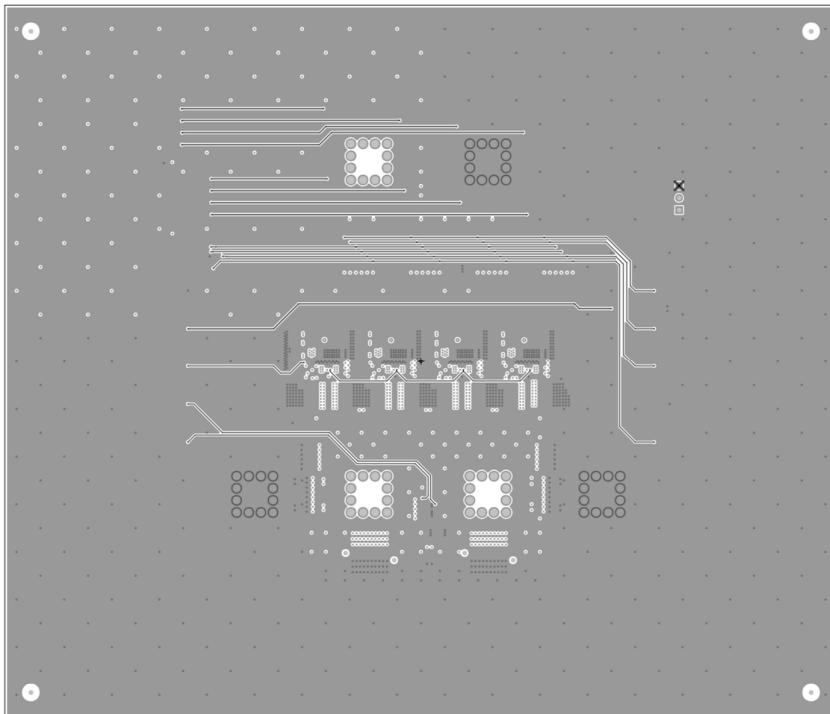


Figure 8 Board layout – layer 6

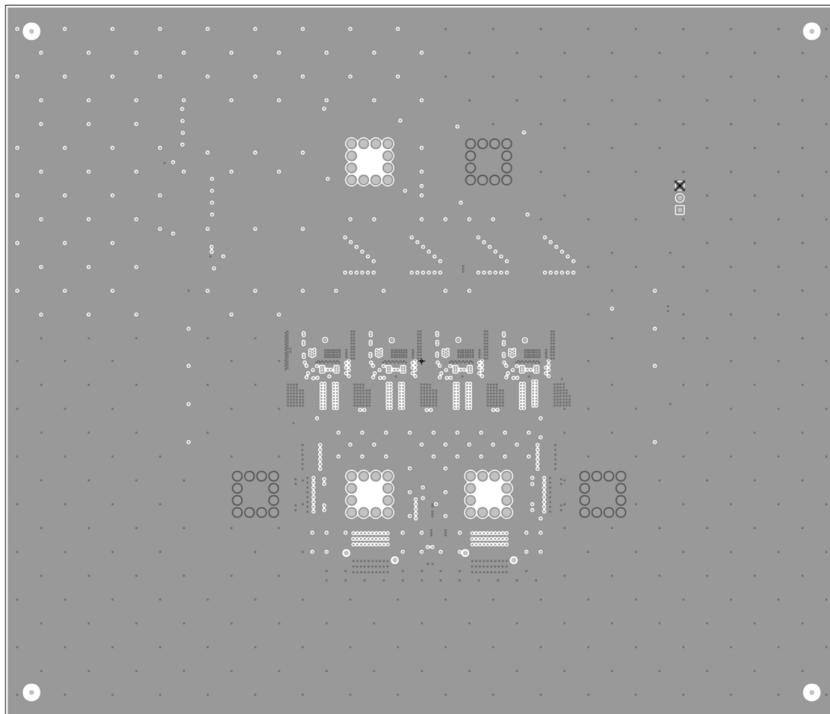


Figure 9 Board layout – layer 7

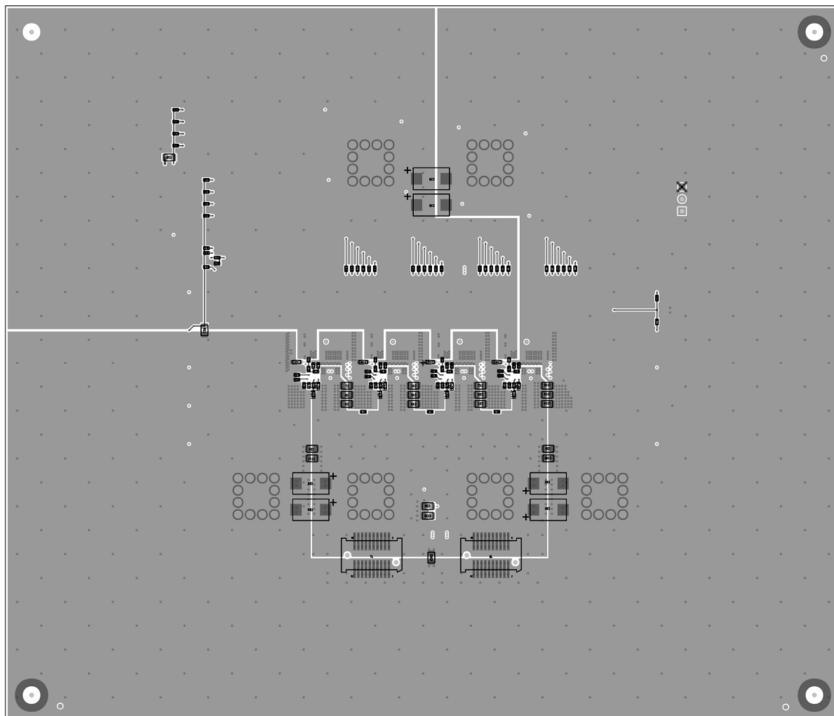


Figure 10 Board layout – layer 8

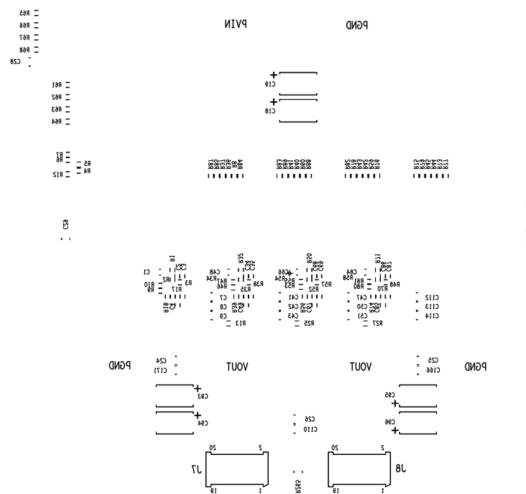


Figure 11 Board layout – silkscreen Bottom

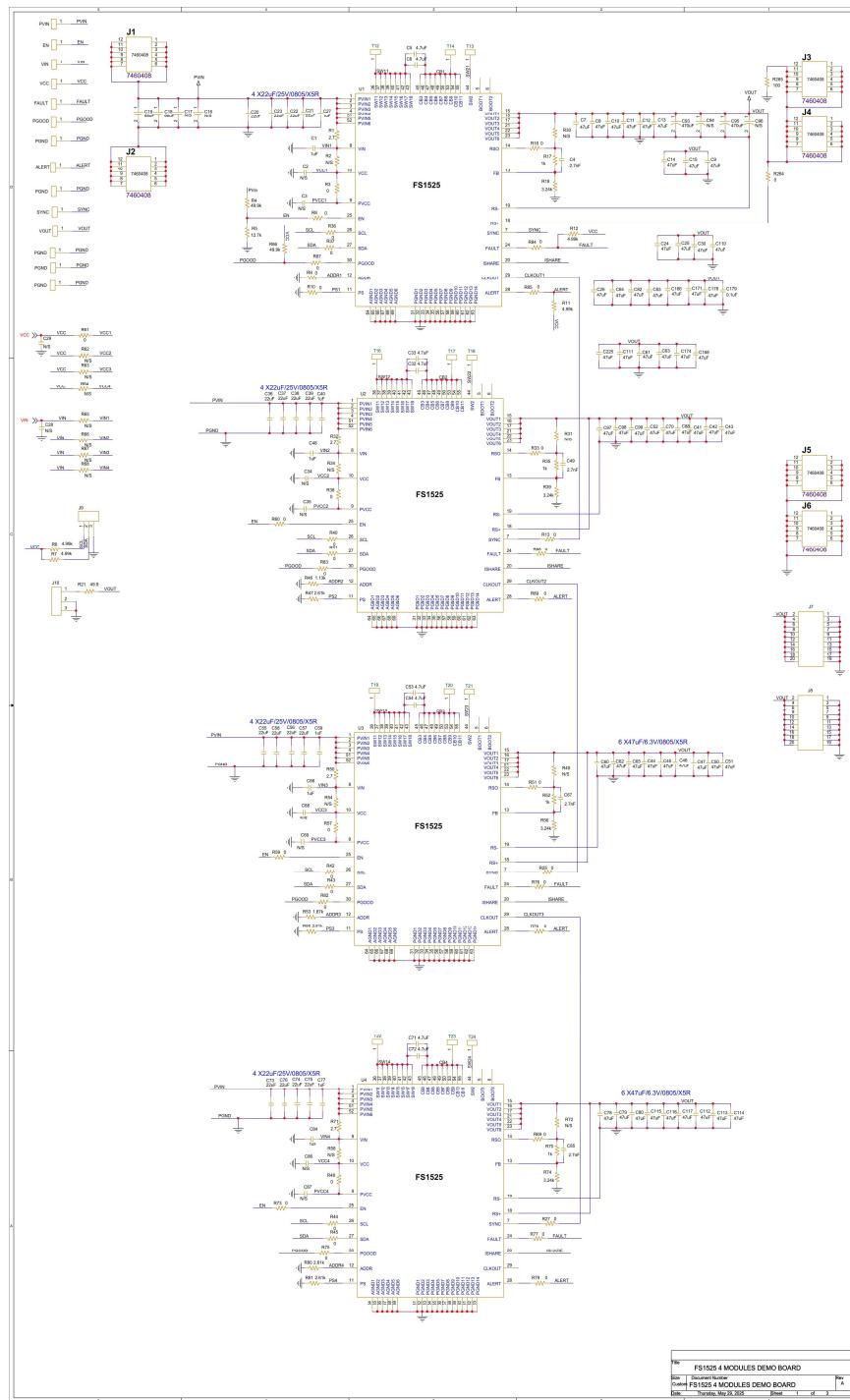


Figure 12 Schematic

V_{OUT} (V)	R_{TOP}/R_{BOTTOM}	V_{OUT} (V)	R_{TOP}/R_{BOTTOM}
0.65	0.0617	1	0.6494
0.7	0.1468	1.05	0.7299
0.72	0.1779	1.1	0.8065
0.8	0.3086	1.2	0.9804
0.85	0.3922	1.25	1.0741
0.9	0.4762	1.5	1.4684
0.95	0.5618	1.8	1.9569

Table 1 Resistor Divider Ratio for Different Output Voltages.

*NOTE – Modify R18, R39, R56 & R74 (RBOTTOM) for different VOUT as per the included table. R17, R35, R52 & R70 = 1 kΩ (RTOP) & C9, C49, C67 & C85 = 2700pF is recommended. For VOUT = 0.6V; R17, R35, R52 & R70 = 0Ω, C9, C49, C67 & C85 = DNP.

PS Resistor: R10 = 0Ω for 0.6V = $V_{OUT} \leq 0.9V$; for $0.9V < V_{OUT} < 1.2V$, R10 = 8.66k; and R10 = 7.87k for $V_{OUT} \geq 1.2V$

Item	Quantity	Reference	Description
1	4	C1,C48,C66,C84	1uF/0603/25V/X7R
2	4	C27,C40,C59,C77	1uF/0402/25V/X7R
4	8	C5,C6,C32,C33,C53,C54,C71,C72	4.7uF/0805/16V/X7R
6	53	C7,C8,C9,C10,C11,C12,C13,C14,C15,C24,C25,C26,C30,C41,C42,C43,C44,C45,C46,C47,C50,C51,C52,C60,C61,C62,C63,C64,C65,C70,C78,C79,C80,C82,C83,C88,C97,C98,C99,C110,C111,C112,C113,C114,C115,C116,C117,C166,C168,C171,C174,C178,C225	47uF/0805/6.3V/X5R
7	16	C20,C21,C22,C23,C36,C37,C38,C39,C55,C56,C57,C58,C73,C74,C75,C76	22uF/0805/25V/X5R
9	2	C18,C19	68uF, 25V, poscap
10	2	C93,C95	470uF, ESR 3mohm
11	4	C4,C49,C67,C85	2.7nF/0402
		C179	0.1uF/0805/25V/X7R
12	14	T1,T2,T3,T4,T5,T6,T7,T9,T10,T15,T25,T26,T27,T49	PC TEST POINT COMPACT
13	6	J1,J2,J3,J4,J5,J6	Terminals
14	1	J10	CONN U.FL RCPT STR 50 OHM SMD
		J9	CON3
16	39	R3,R8,R9,R13,R16,R25,R27,R33,R36,R37,R38,R40,R41,R42,R43,R44,R45,R48,R51,R57,R59,R60,R61,R69,R73,R75,R76,R77,R78,R79,R82,R83,R84,R85,R87,R88,R89,R264,R10	0/0402
17	2	R4,R86	49.9k/0402
18	1	R5	12.7k/0402
19	4	R6,R7,R11,R12	4.99k/0402
20	4	R17,R35,R52,R70	1k/0402
21	1	R21	49.9/0402
22	1	R46	1.13k/0402
23	1	R53	1.87k/0402
24	4	R47,R55,R80,R81	2.61k/0402
29	4	R18,R39,R56,R74	3.24k/0402
		R265	100
30	4	U1,U2,U3,U4	FS1525

Table 2 4-Module Board Bill of Material

Typical performance

Figure 13 to Figure 22 show typical operating waveforms for the evaluation board, while Figure 26 shows a thermal image of the board in operation. In all cases, the board is operating at room temperature with no airflow; P_{VIN} is 12V, V_{OUT} is 0.8V and I_o is 0–100A.

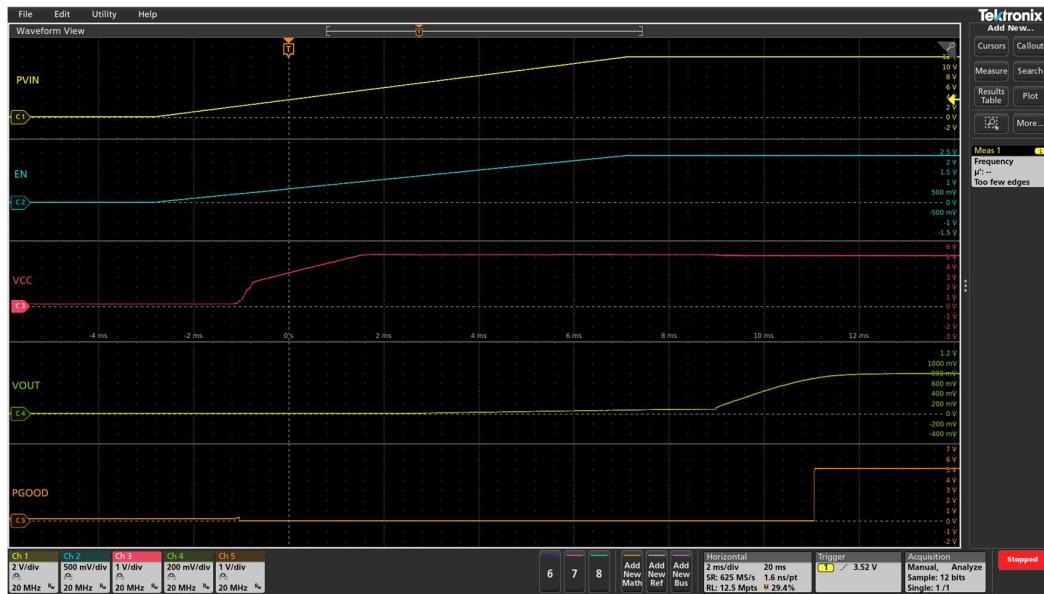


Figure 13 Startup with no load (Ch1: P_{VIN} , Ch2: Enable, Ch3: V_{CC} , Ch4: V_{OUT} , Ch5: PGood)

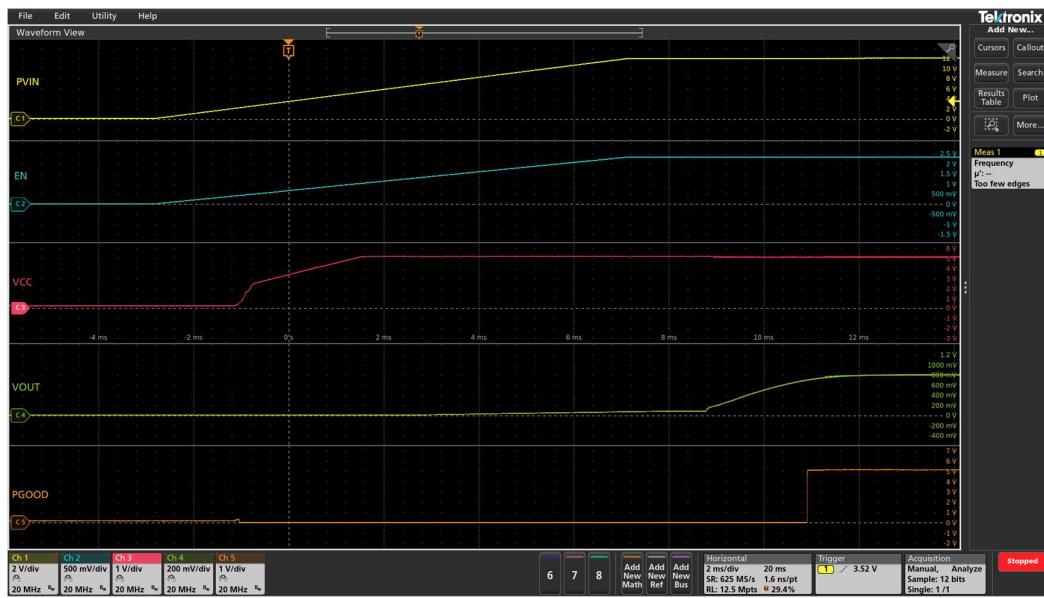


Figure 14 Startup with 100A load (Ch1: P_{VIN} , Ch2: Enable, Ch3: V_{CC} , Ch4: V_{OUT} , Ch5: PGood)

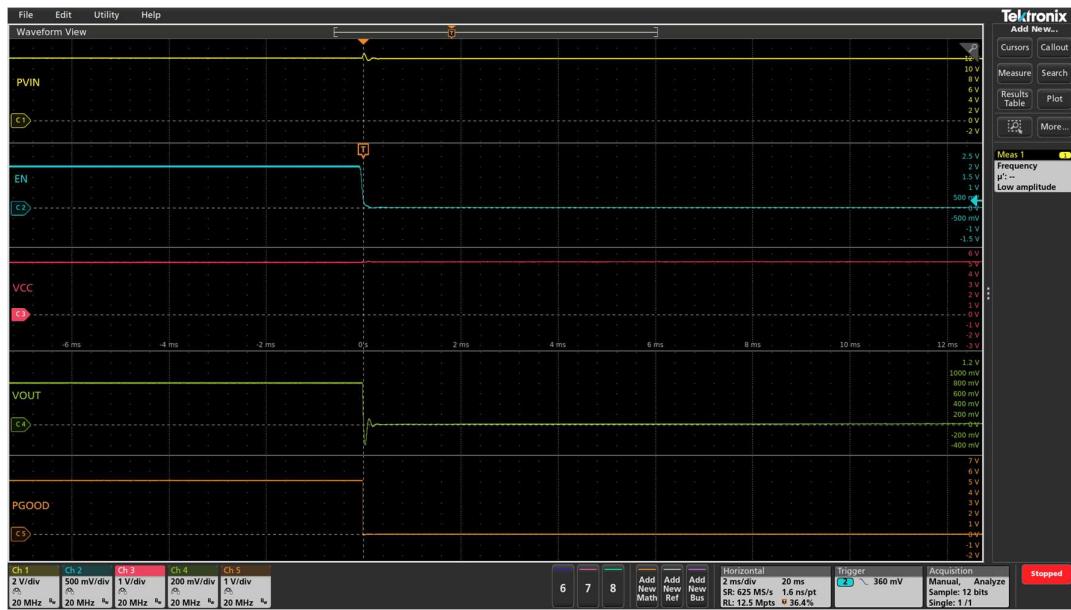


Figure 15 Shutdown with Enable de-assertion at 100A load
(Ch1:PV_{IN}, Ch2: Enable, Ch3: V_{CC}, Ch4: V_{OUT}, Ch5: PGood)



Figure 16 Switch node waveforms at no load



Figure 17 Switch node waveforms at 100A



Figure 18 OCP Recovery to 100A (Ch1:PV_{IN}, Ch2: Enable, Ch3: V_{CC}, Ch4: V_{OUT}, Ch5: PGood)

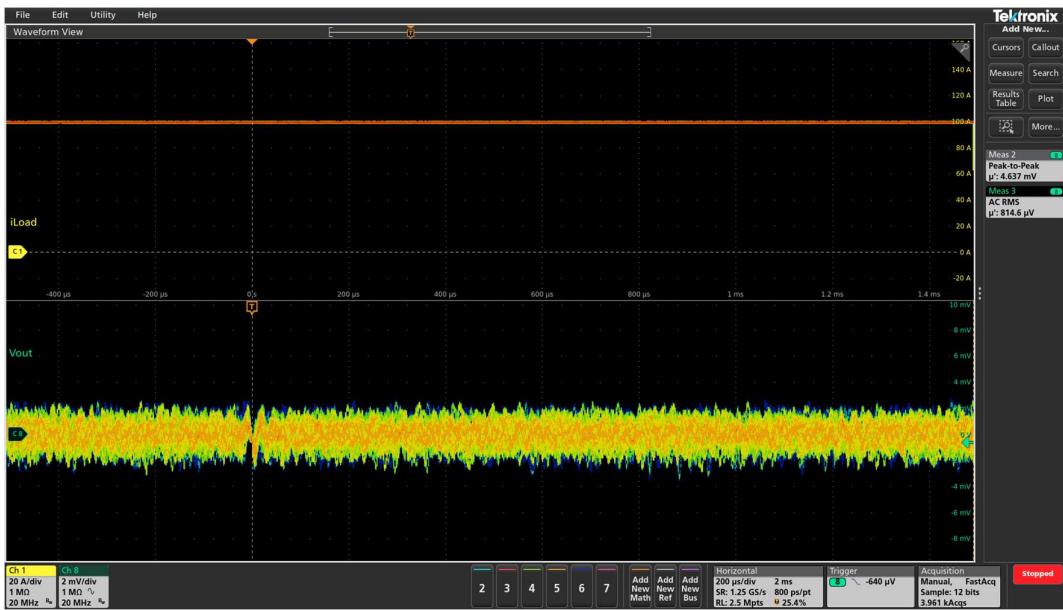


Figure 19 Vout Ripple(100A)

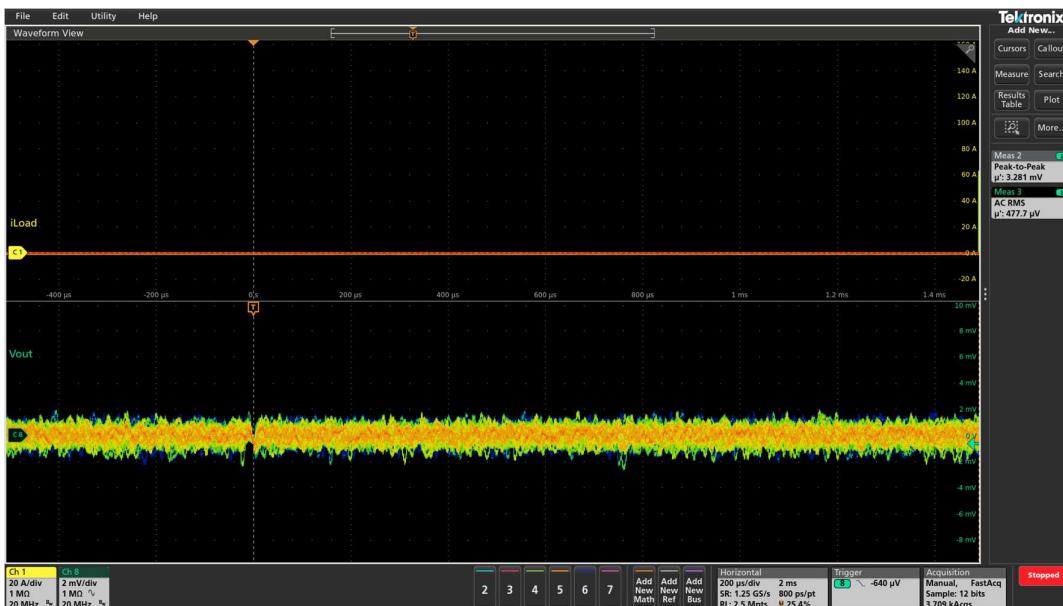


Figure 20 Vout Ripple(0A)

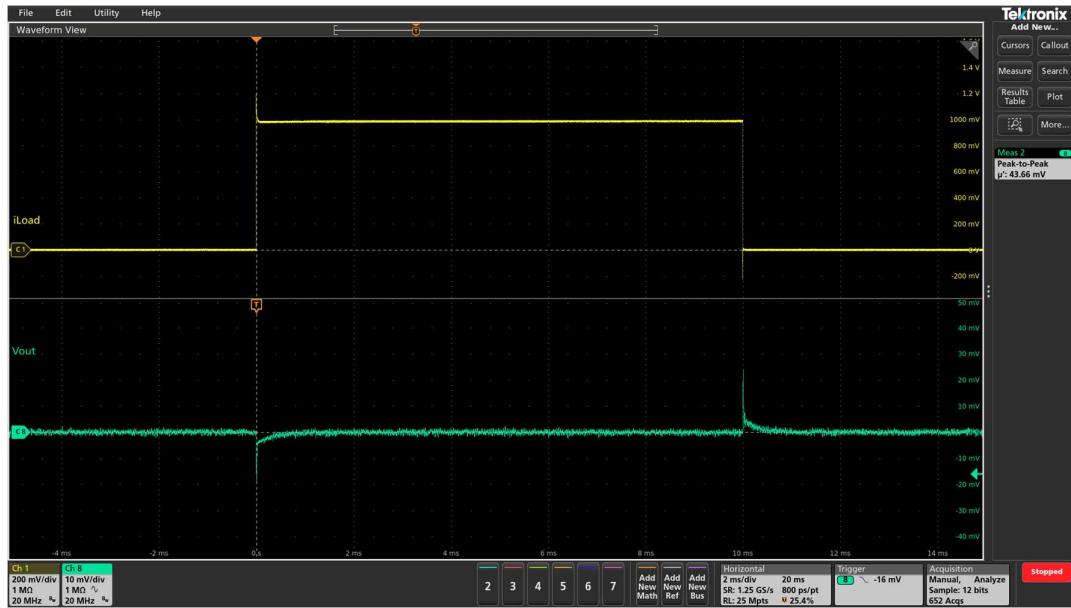


Figure 21 Transient response 0A to 20A (Ch1: i_{OUT} , Ch8: V_{OUT}), peak-peak deviation = 43.66mV, load slew rate = 100A/ μ s

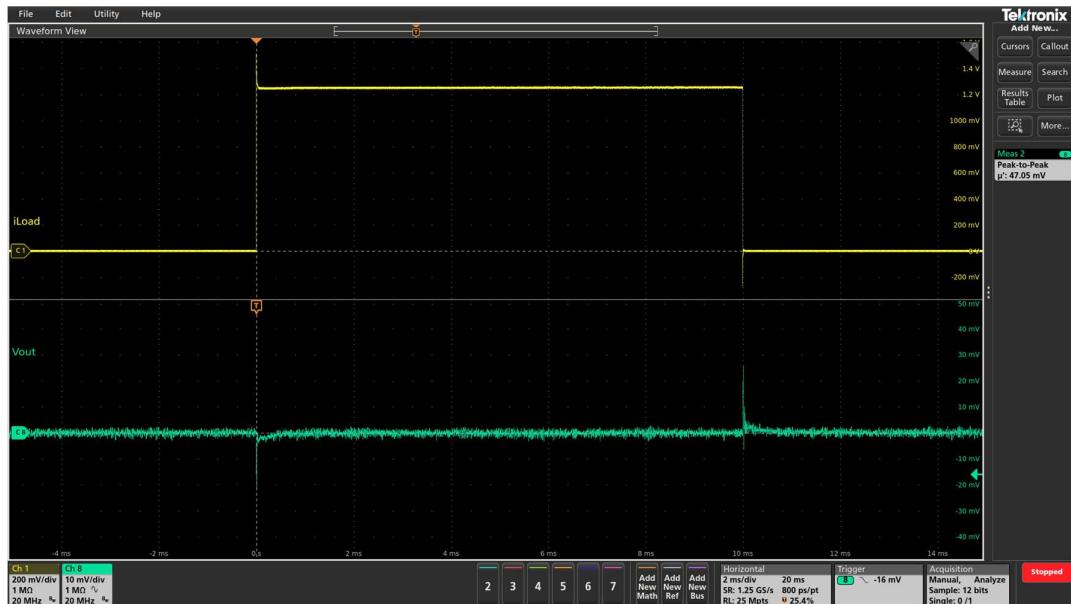


Figure 22 Transient response 50A to 75A (Ch1: i_{OUT} , Ch8: V_{OUT}), peak-peak deviation = 47.05mV, load slew rate = 100A/ μ s

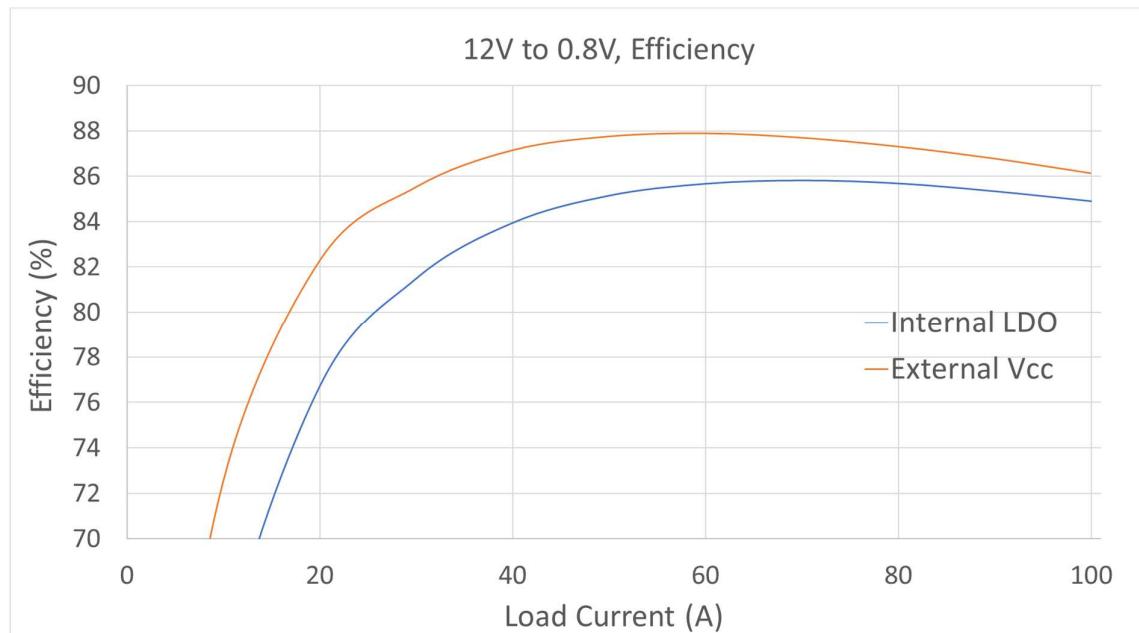


Figure 23 Efficiency

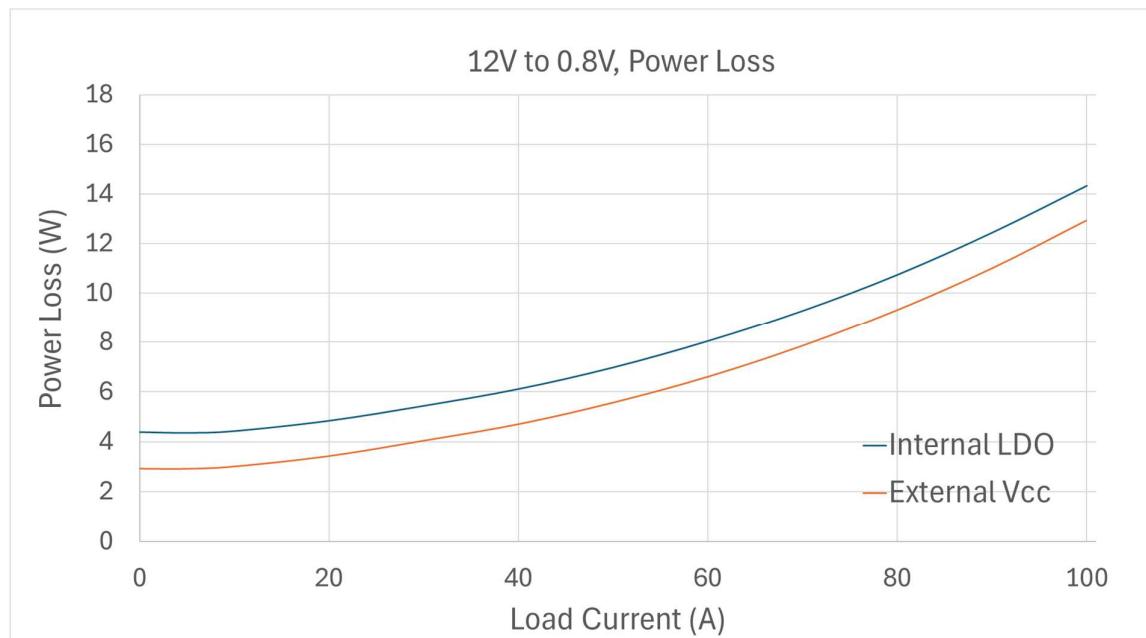


Figure 24 Power loss

NOTE – For External Vcc Connection, Remove R1,R32, Install R2, R34 = 0 ohm & C2, C3, C50, C51 = 2.2 μ F (10V 0402)

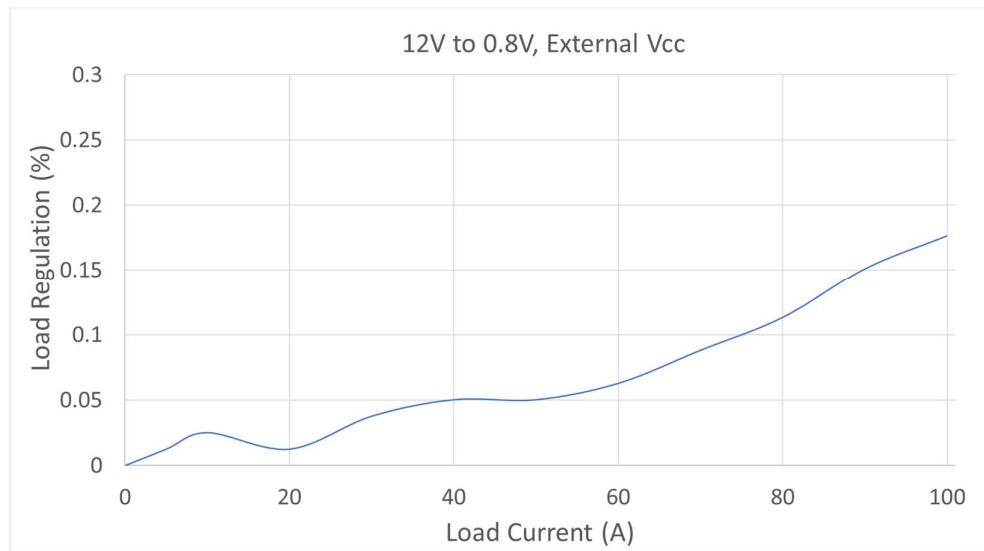


Figure 25 Load regulation ($I_o = 0$ –100A)

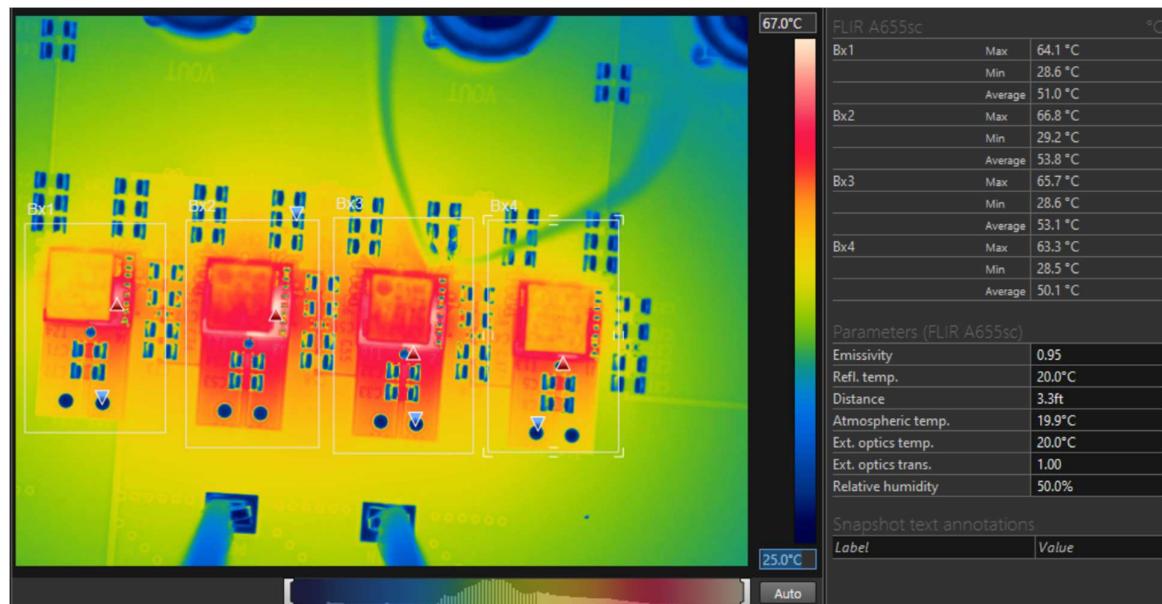


Figure 26 Thermal image at $P_{V_{IN}} = 12V$, $V_{OUT} = 0.8V$, $I_o = 100A$, room temperature, no airflow, External Vcc (5V), FS1525 maximum temperature rise = 41.8°C

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