

TDK Power Strip Sequencer 1

General Description

Dialog SLG7TD43741 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

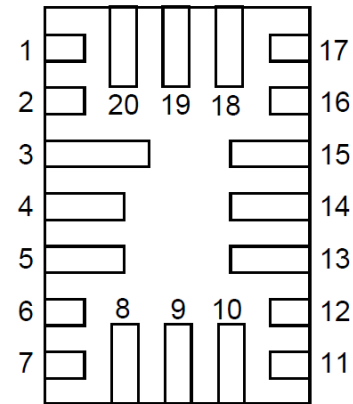
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

5 Outputs - Push Pull 1X

Pin Configuration

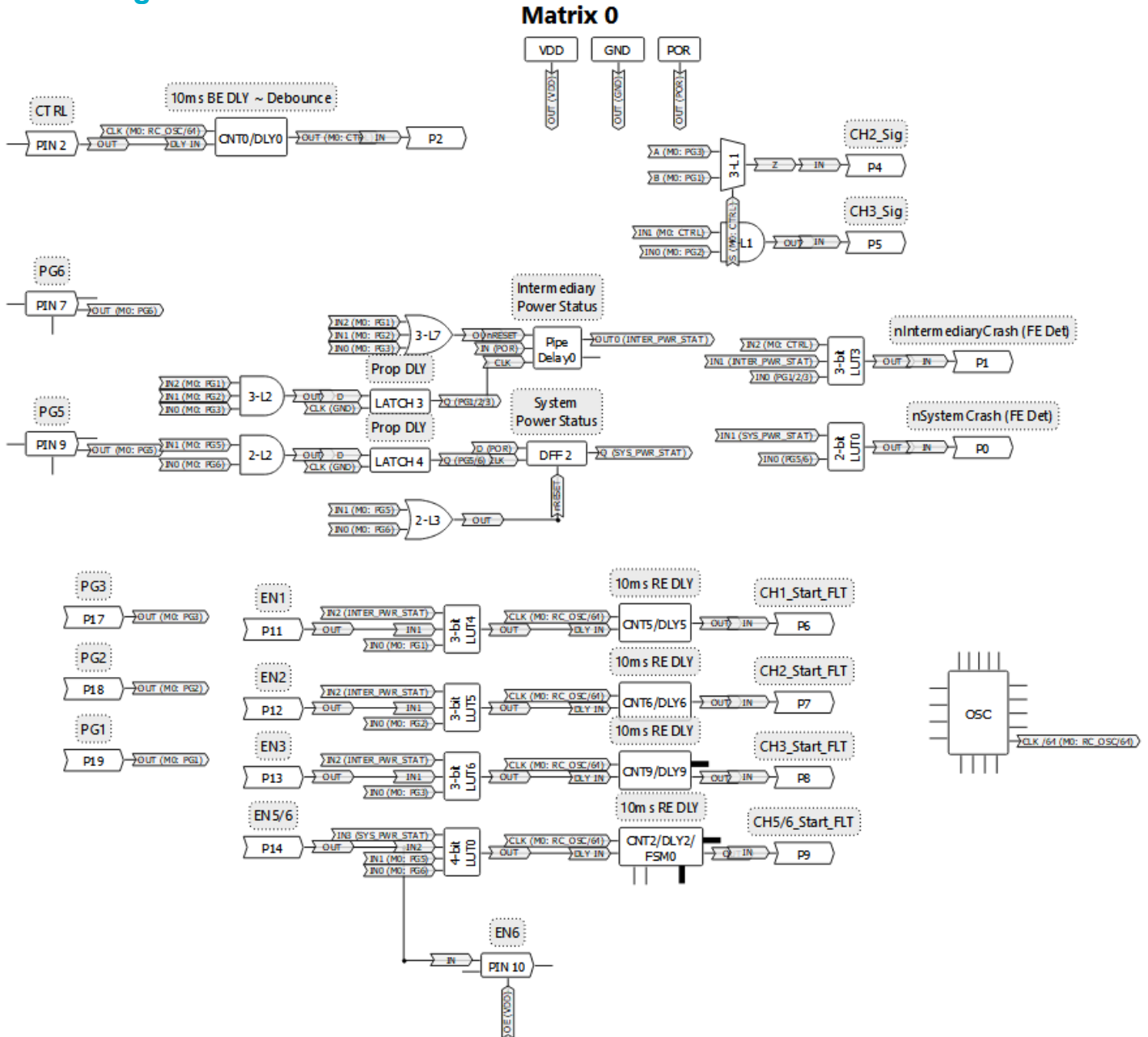


**STQFN-20
(Top View)**

Pin name

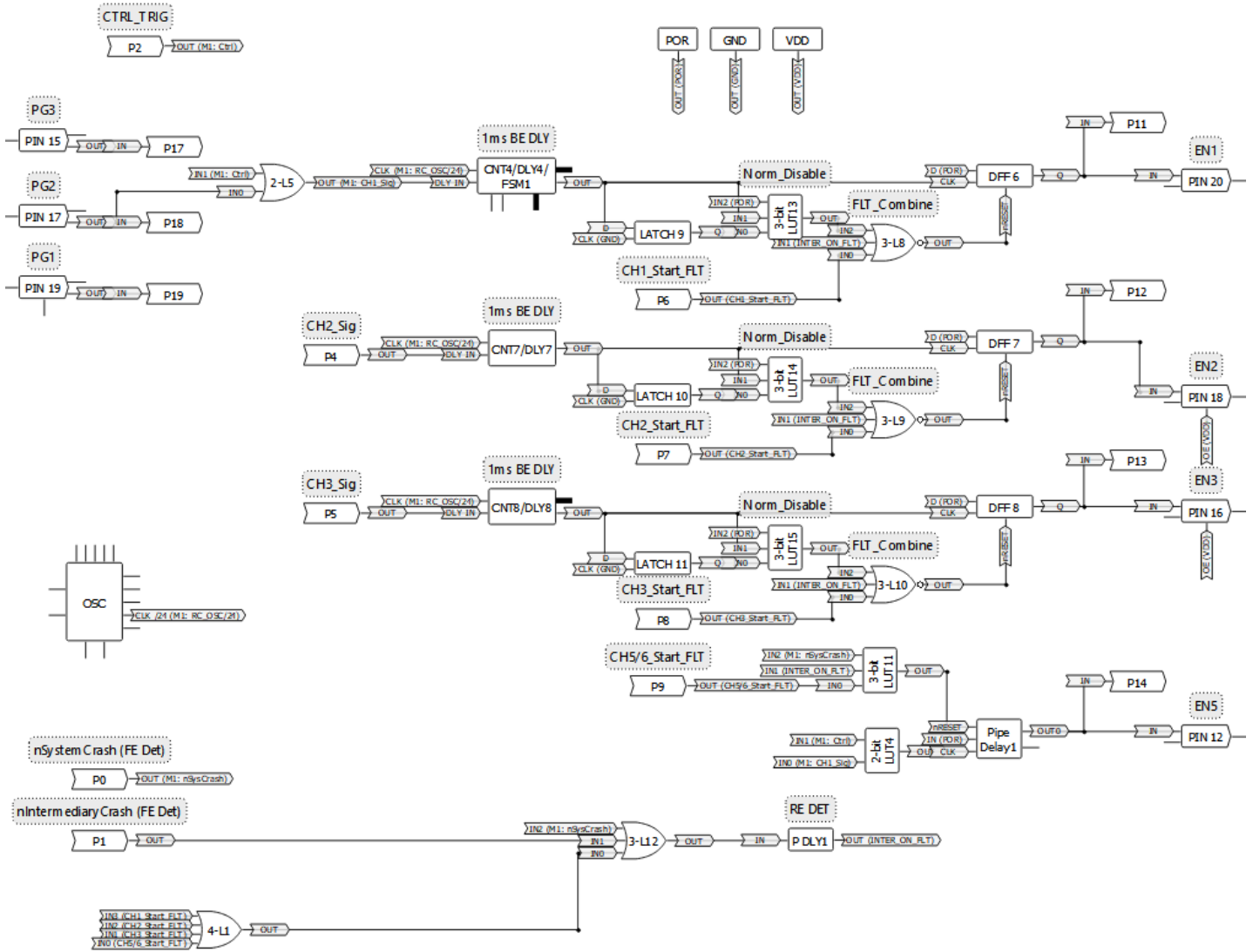
Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	CTRL	12	EN5
3	NC	13	NC
4	NC	14	NC
5	NC	15	PG3
6	NC	16	EN3
7	PG6	17	PG2
8	NC	18	EN2
9	PG5	19	PG1
10	EN6	20	EN1

Block Diagram



TDK Power Strip Sequencer 1

Matrix 1



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	CTRL	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	NC	--	Keep Floating or Connect to GND	--
4	NC	--	Keep Floating or Connect to GND	--
5	NC	--	Keep Floating or Connect to GND	--
6	NC	--	Keep Floating or Connect to GND	--
7	PG6	Digital Input	Digital Input with Schmitt trigger	floating
8	NC	--	Keep Floating or Connect to GND	--
9	PG5	Digital Input	Digital Input with Schmitt trigger	floating
10	EN6	Digital Output	Push Pull 1X	floating
11	GND	GND	Ground	--
12	EN5	Digital Output	Push Pull 1X	floating
13	NC	--	Keep Floating or Connect to GND	--
14	NC	--	Keep Floating or Connect to GND	--
15	PG3	Digital Input	Digital Input with Schmitt trigger	floating
16	EN3	Digital Output	Push Pull 1X	floating
17	PG2	Digital Input	Digital Input with Schmitt trigger	floating
18	EN2	Digital Output	Push Pull 1X	floating
19	PG1	Digital Input	Digital Input with Schmitt trigger	floating
20	EN1	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7TD43741V	20-pin STQFN
SLG7TD43741VTR	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	10	mA
Current at Input Pin		-1.0	1.0	mA
Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.39	nA
	Vin = VDD	--	142.92	
Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.24	nA
	Vin = VDD	--	143.85	
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		3	3.3	3.6	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	VDD = 3.6V; All Inputs LOW	--	1	--	µA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	45	mA
		T _J = 110°C	--	--	21	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	69	mA
		T _J = 110°C	--	--	33	mA
V _{IH}	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	1.949	--	VDD	V
		Logic Input with Schmitt Trigger at VDD=3.3V	2.239	--	VDD	V
V _{IL}	LOW-Level Input Voltage	Logic Input at VDD=3.3V	0	--	1.286	V
		Logic Input with Schmitt Trigger at VDD=3.3V	0	--	1.150	V
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, IOH=3mA at VDD=3.3V	2.713	3.095	--	V
V _{OL}	LOW-Level Output Voltage	Push-Pull 1X, IOL=3mA, at VDD=3.3V	--	0.148	0.228	V
I _{OH}	HIGH-Level Output Current	Push-Pull 1X, VOH=2.4V at VDD=3.3V	5.608	10.774	--	mA
I _{OL}	LOW-Level Output Current	Push-Pull 1X, VOL=0.4V, at VDD=3.3V	4.875	7.795	--	mA
R _{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	666.16	--	1261.68	kΩ

TDK Power Strip Sequencer 1

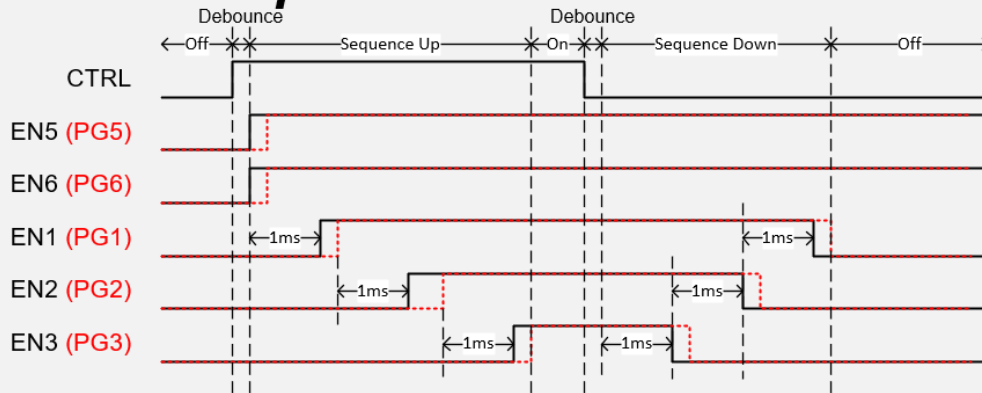
T _{DLY0}	Delay0 Time	At temperature 25°C	9.81	10.02	10.24	ms
		At temperature -40 +85°C	9.48	10.02	10.71	ms
T _{DLY2}	Delay2 Time	At temperature 25°C	9.81	10.02	10.24	ms
		At temperature -40 +85°C	9.48	10.02	10.71	ms
T _{DLY4}	Delay4 Time	At temperature 25°C	0.99	1.02	1.06	ms
		At temperature -40 +85°C	0.95	1.02	1.10	ms
T _{DLY5}	Delay5 Time	At temperature 25°C	9.81	10.02	10.24	ms
		At temperature -40 +85°C	9.48	10.02	10.71	ms
T _{DLY6}	Delay6 Time	At temperature 25°C	9.81	10.02	10.24	ms
		At temperature -40 +85°C	9.48	10.02	10.71	ms
T _{DLY7}	Delay7 Time	At temperature 25°C	0.99	1.02	1.06	ms
		At temperature -40 +85°C	0.95	1.02	1.10	ms
T _{DLY8}	Delay8 Time	At temperature 25°C	0.99	1.02	1.06	ms
		At temperature -40 +85°C	0.95	1.02	1.10	ms
T _{DLY9}	Delay9 Time	At temperature 25°C	9.81	10.02	10.24	ms
		At temperature -40 +85°C	9.48	10.02	10.71	ms
T _{SU}	Startup Time (see Note 3)	From VDD rising past P _{ON} _{THR}	0.660	1.4	3.740	ms
P _{ON} _{THR}	Power On Threshold	V _{DD} Level Required to Start Up the Chip	0.953	1.462	1.707	V
P _{OFF} _{THR}	Power Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V

Note:

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
3. VDD ramp rising speed must be less than 0.6 V/μs after power on. Violating this specification may cause chip to restart.

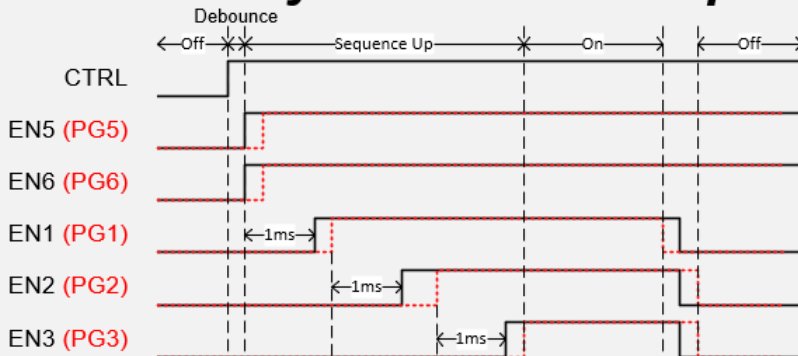
Timing Diagram

Normal Sequence:

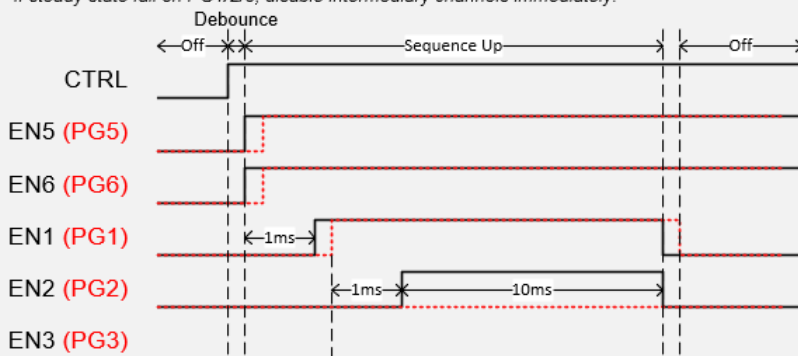


Note:
 The **black** signals represent the enable outputs for each channel.
 The **red** signals represent the power good inputs for each channel.

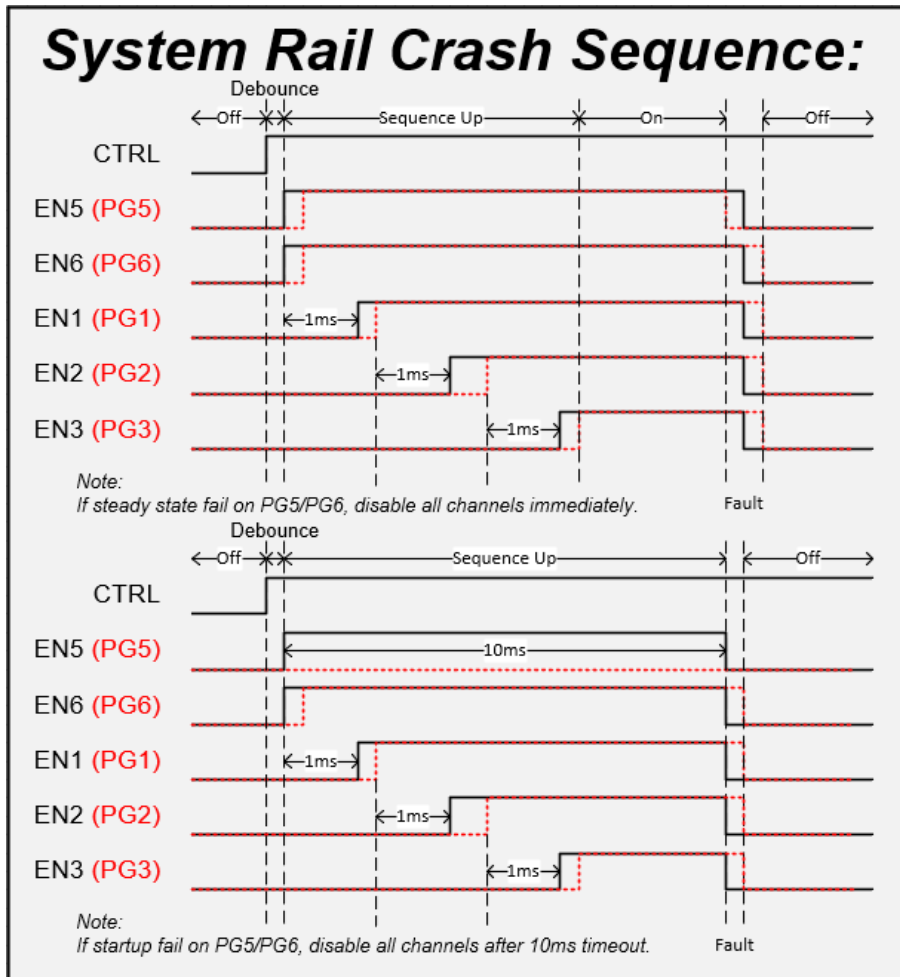
Intermediary Rail Crash Sequence:



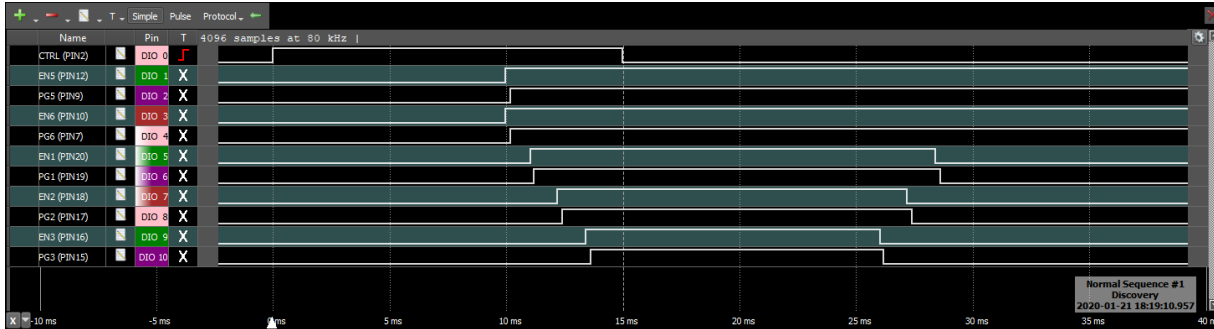
Note:
 If steady state fail on PG1/2/3, disable intermediary channels immediately. Fault



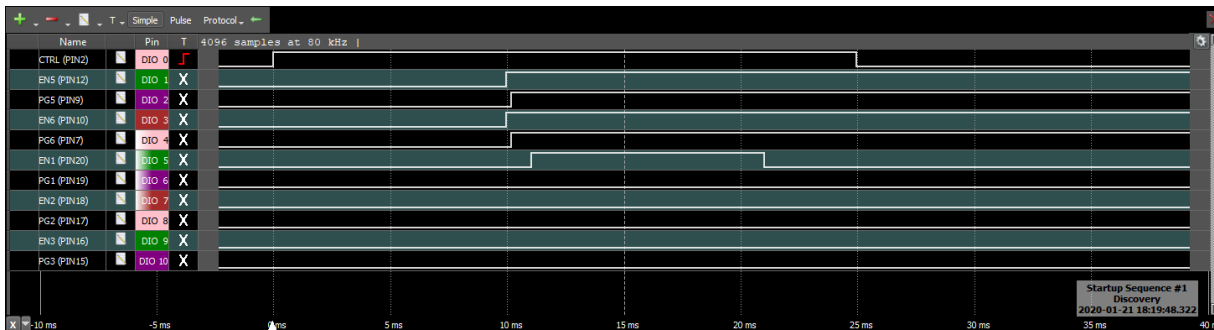
Note:
 If startup fail on PG1/2/3, disable intermediary channels after 10ms timeout. Fault



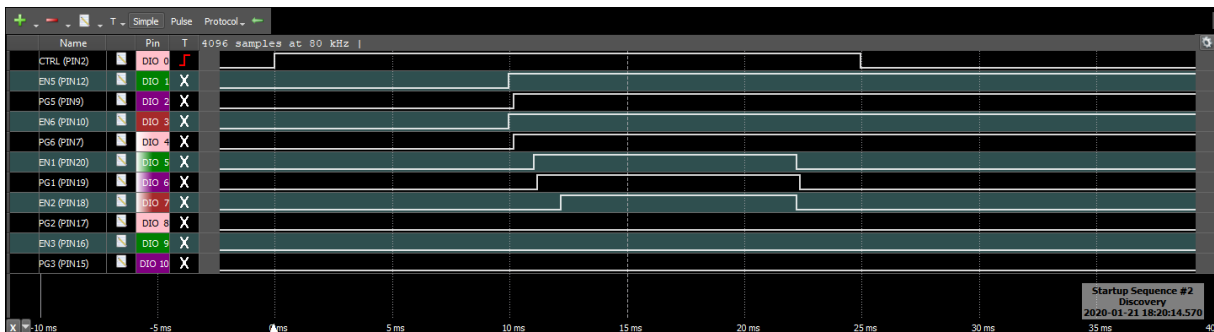
Functionality Waveforms



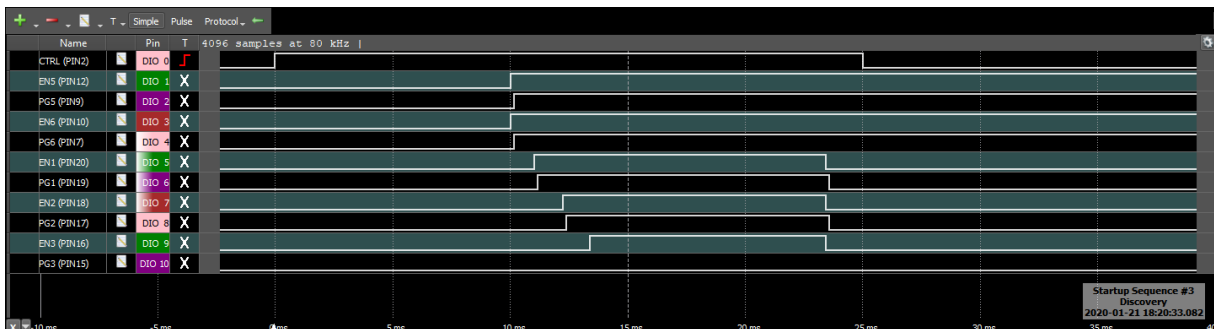
Waveform 1: Normal Sequence



Waveform 2: Startup Sequence #1 Behavior (CH1 Fault)

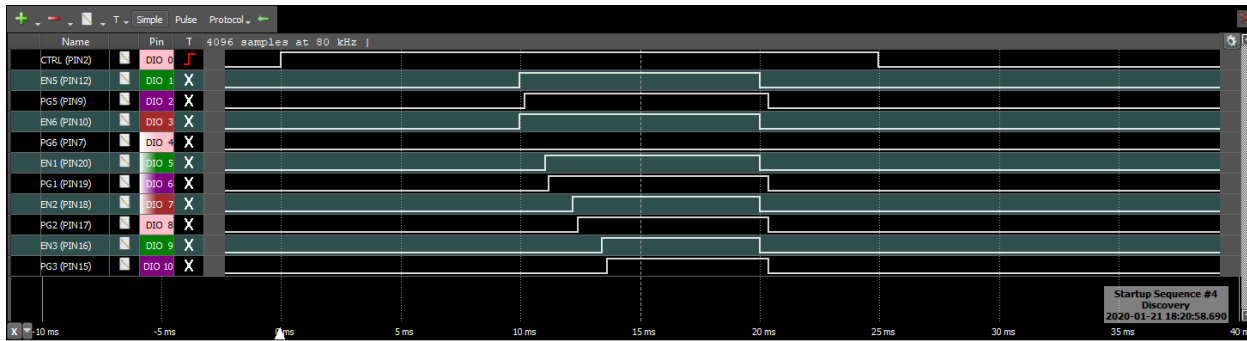


Waveform 3: Startup Sequence #2 Behavior (CH2 Fault)

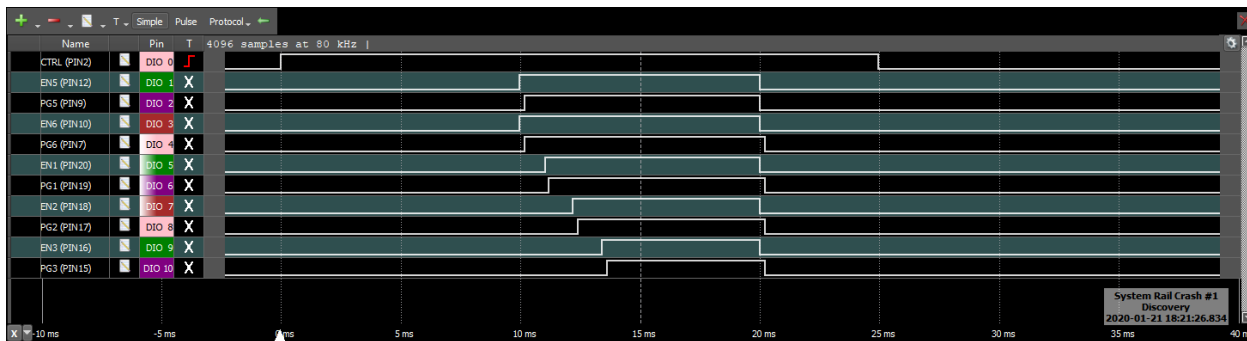


Waveform 4: Startup Sequence #3 Behavior (CH3 Fault)

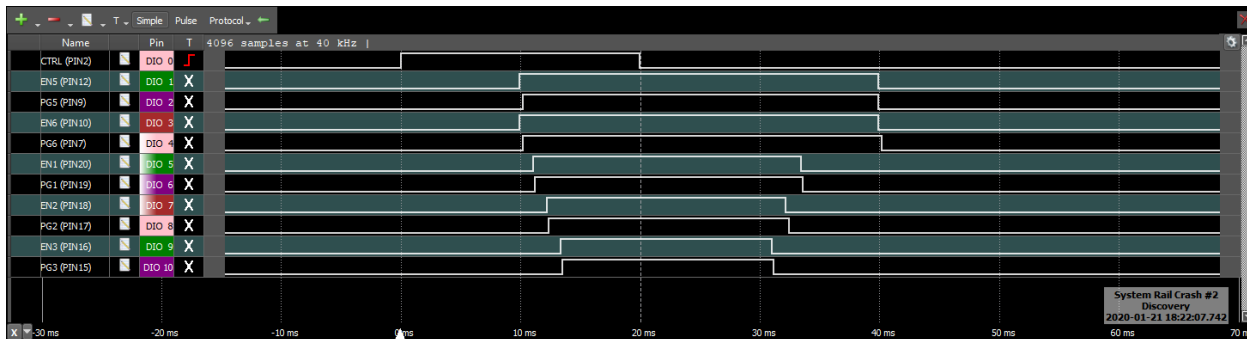
TDK Power Strip Sequencer 1



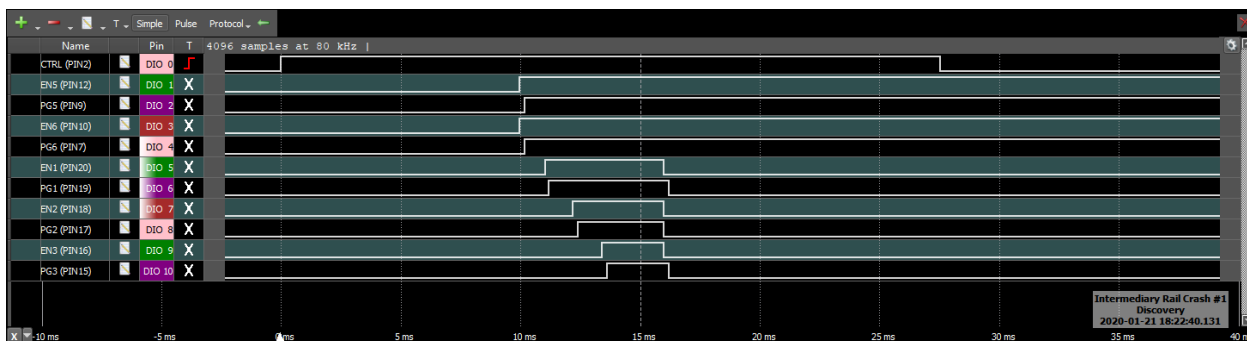
Waveform 5: Startup Sequence #4 Behavior (CH6 Fault)



Waveform 6: System Rail Crash #1 Behavior (CH5 Fault)



Waveform 7: System Rail Crash #2 Behavior (CH5 Fault)



Waveform 8: Intermediary Rail Crash #1 Behavior (CH2 Fault)

Package Top Marking



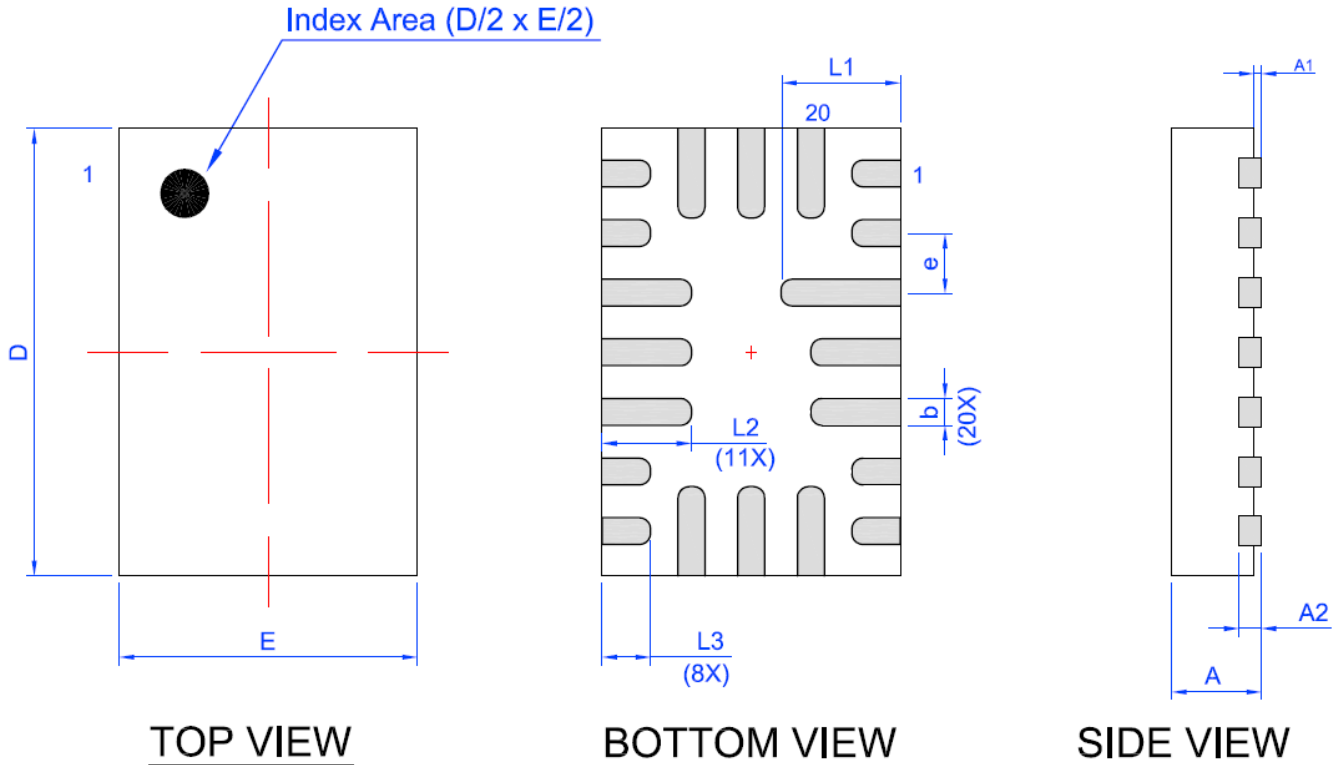
Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.14	005	U	0x84286400			01/21/2020

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

TDK Power Strip Sequencer 1

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

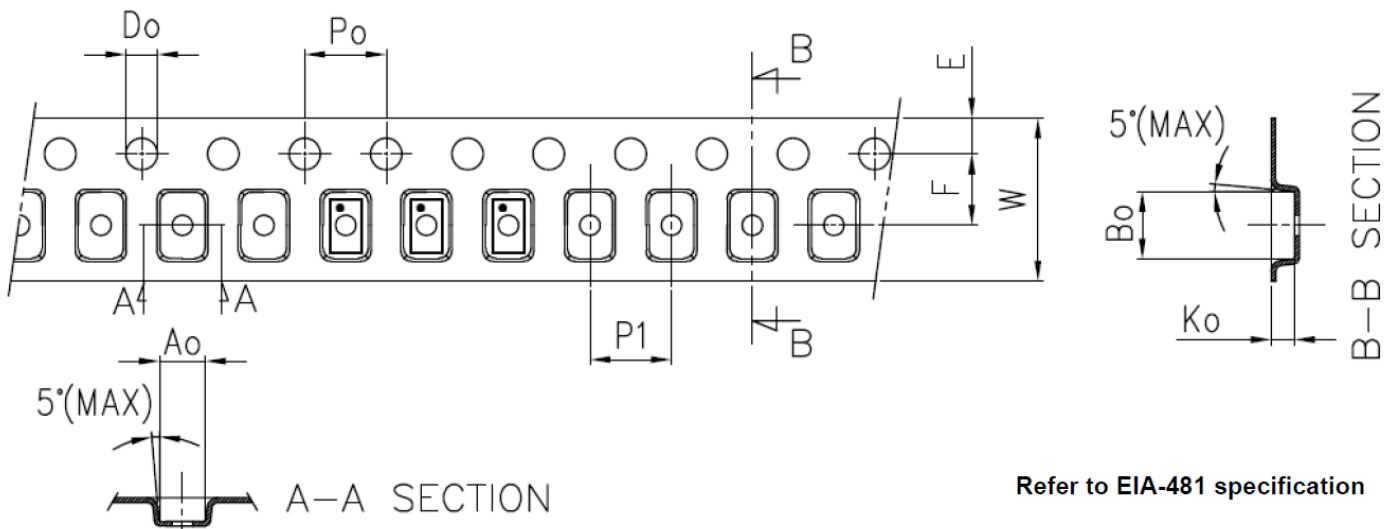
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3 mm 0.4P COL	20	2 x 3 x 0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P COL	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

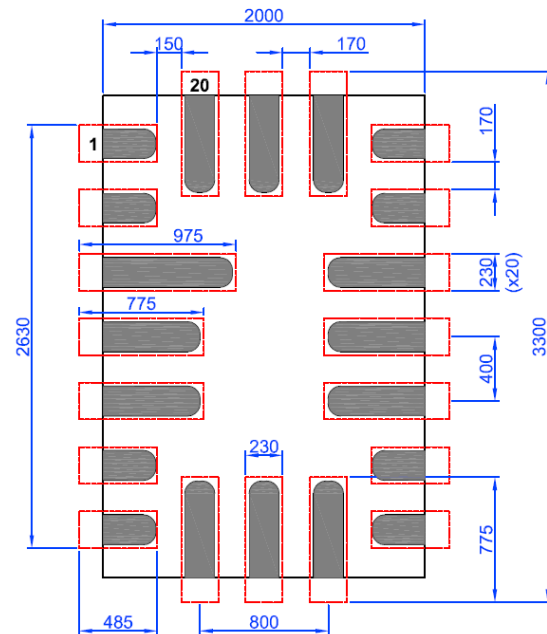
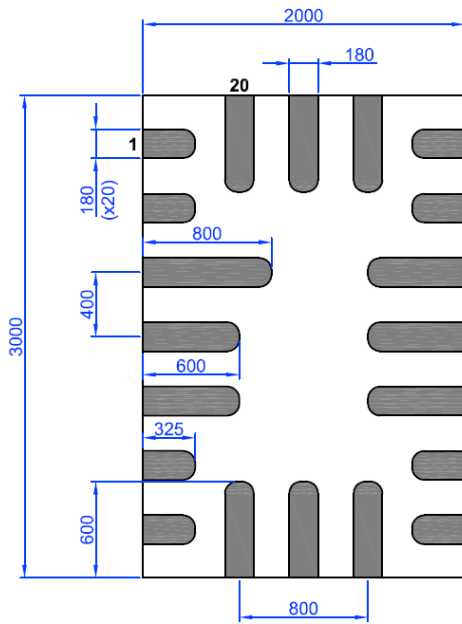
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm³ (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: μm



Datasheet Revision History

Date	Version	Change
11/21/2019	0.10	New design for SLG46620V chip
11/21/2019	0.11	Changed design
12/20/2019	0.12	Added Features: Startup fault sequence detection Modified Features: Pinout change, Immediate rail crashes upon steady state faults
01/10/2020	0.13	Modified Pinout, Added Debounce on CTRL, Remove Pull Up Resistors
01/21/2020	0.14	Removed EN2/EN3 startup dependency on EN5&EN6

Disclaimer

Information in this document is believed to be accurate and reliable. However, Dialog Semiconductor does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. Dialog Semiconductor furthermore takes no responsibility whatsoever for the content in this document if provided by any information source outside of Dialog Semiconductor.

Dialog Semiconductor reserves the right to change without notice the information published in this document, including without limitation the specification and design of the related semiconductor products, software and applications.

Applications, software, and semiconductor products described in this document are for illustrative purposes only. Dialog Semiconductor makes no representation or warranty that such applications, software and semiconductor products will be suitable for the specified use without further testing or modification. Unless otherwise agreed in writing, such testing or modification is the sole responsibility of the customer and Dialog Semiconductor excludes all liability in this respect.

Customer notes that nothing in this document may be construed as a license for customer to use the Dialog Semiconductor products, software and applications referred to in this document. Such license must be separately sought by customer with Dialog Semiconductor.

All use of Dialog Semiconductor products, software and applications referred to in this document are subject to Dialog Semiconductor's [Standard Terms and Conditions of Sale](http://www.dialog-semiconductor.com), available on the company website (www.dialog-semiconductor.com) unless otherwise stated.

Dialog and the Dialog logo are trademarks of Dialog Semiconductor plc or its subsidiaries. All other product or service names are the property of their respective owners.
© 2019 Dialog Semiconductor. All rights reserved.

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request

Contacting Dialog Semiconductor

United Kingdom (Headquarters)

Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

North America

Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Hong Kong

Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

China (Shenzhen)

Dialog Semiconductor China
Phone: +86 755 2981 3669

Germany

Dialog Semiconductor GmbH
Phone: +49 7021 805-0

Japan

Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Korea

Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shanghai)

Dialog Semiconductor China
Phone: +86 21 5424 9058

The Netherlands

Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Taiwan

Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Email:

enquiry@diasemi.com

Web site:

www.dialog-semiconductor.com