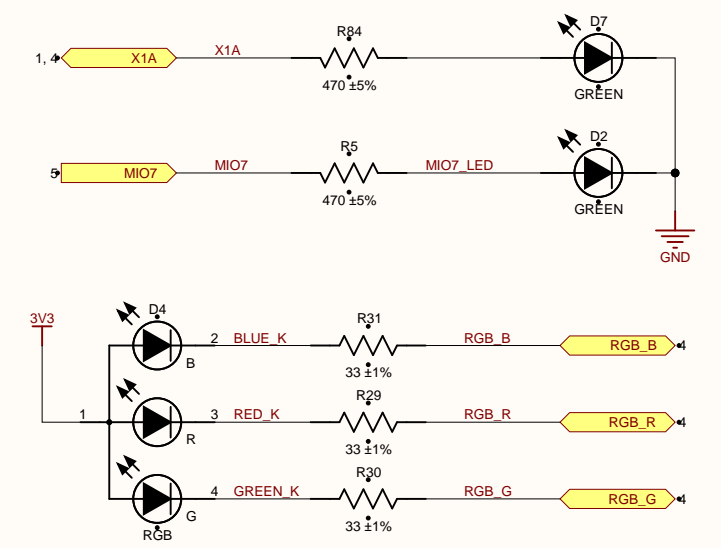
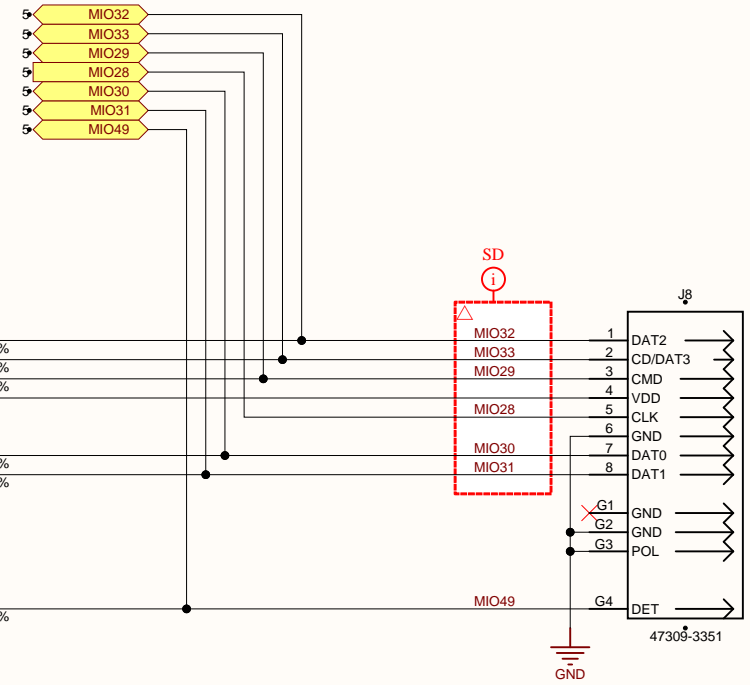
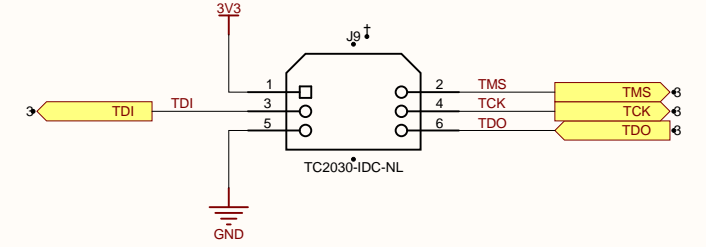
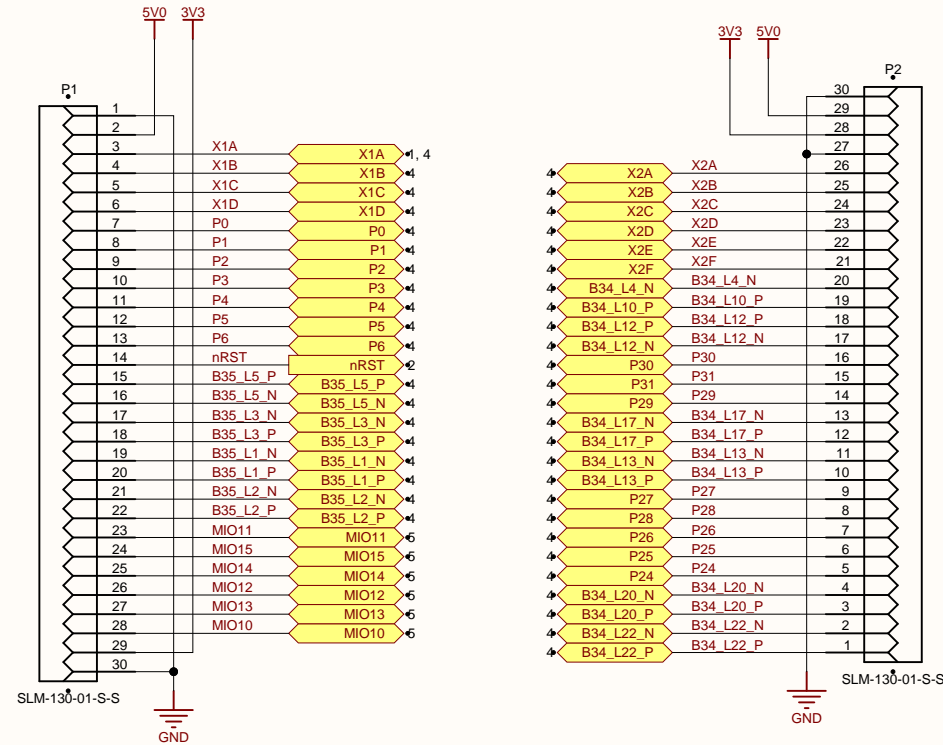


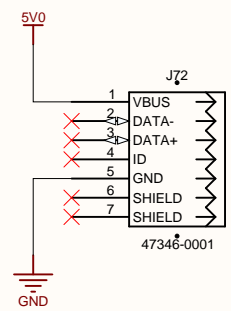
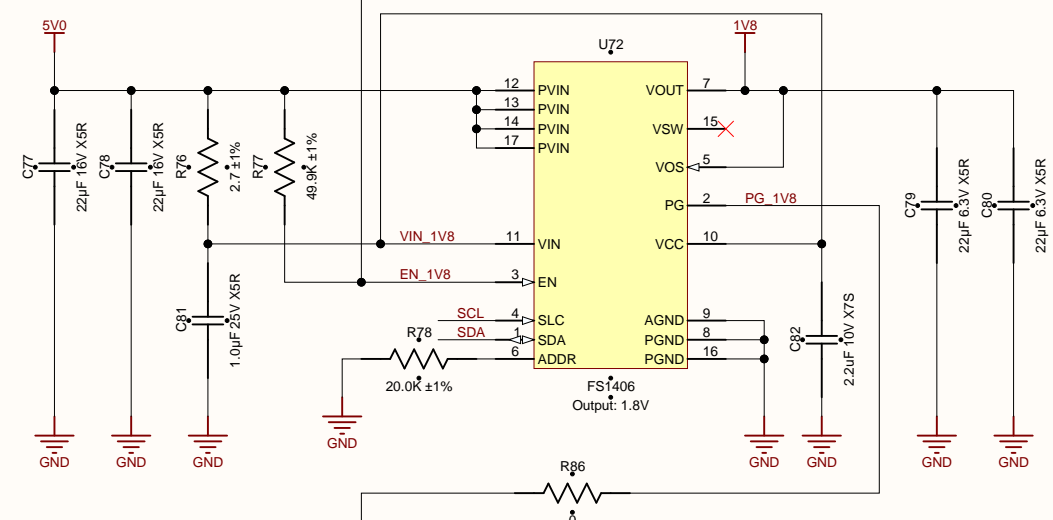
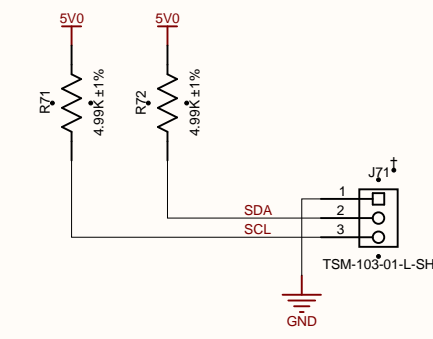
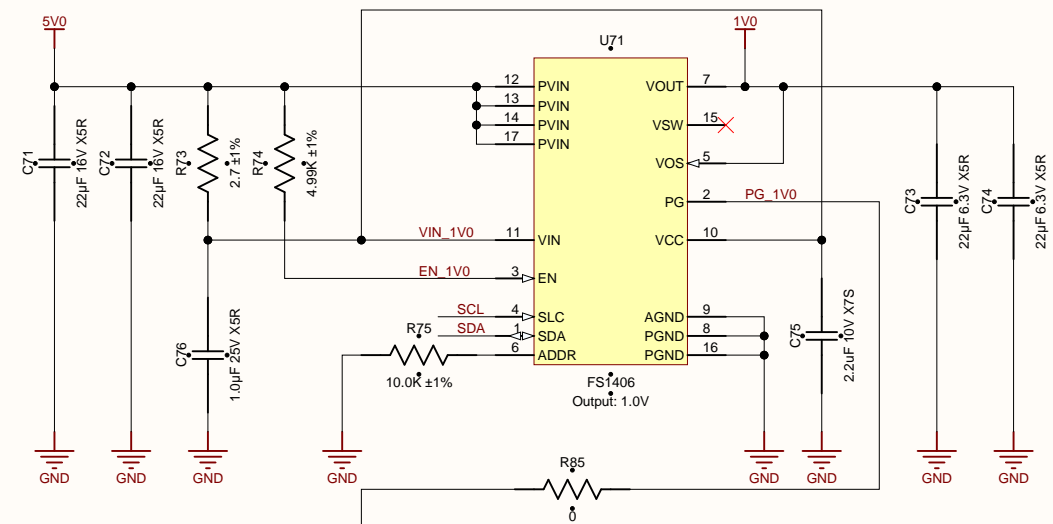


CHANGE NOTES:  
Rev 1, Initial Design



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		PROJECT <b>TDK Zynq 7K Reference</b>	CLIENT PCBA TBD Rev 1
Title: <b>Cover Sheet and Connectors</b>		Morewood Design Labs, Inc. 5001 Baum Blvd. Suite 675 Pittsburgh, PA 15213 412-687-1110	
Size: B	Number: TBD	Rev 1	Stage FF
Date: 1/2/2020	Sheet 1	of 5	
File: Zynq 7K Reference Coversheet.SchDoc		MDL PCB: 20-0001 Fabrication Date:	



### PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is  $V_{CCPINT}$ , then  $V_{CCPAUX}$  and  $V_{CCPLL}$  together, then the PS  $V_{CCO}$  supplies ( $V_{CCO\_MIO0}$ ,  $V_{CCO\_MIO1}$ , and  $V_{CCO\_DDR}$ ) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS\_POR\_B input is required to be asserted to GND during the power-on sequence until  $V_{CCPINT}$ ,  $V_{CCPAUX}$  and  $V_{CCO\_MIO0}$  have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS\_POR\_B timing requirements refer to [Resets](#).

The recommended power-off sequence is the reverse of the power-on sequence. If  $V_{CCPAUX}$ ,  $V_{CCPLL}$ , and the PS  $V_{CCO}$  supplies ( $V_{CCO\_MIO0}$ ,  $V_{CCO\_MIO1}$ , and  $V_{CCO\_DDR}$ ) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering  $V_{CCPLL}$  with the same supply as  $V_{CCPAUX}$ , with an optional ferrite bead filter. Before  $V_{CCPINT}$  reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS\_POR\_B input is asserted to GND, the reference clock to the PS\_CLK input is disabled,  $V_{CCPAUX}$  is lower than 0.70V, or  $V_{CCO\_MIO0}$  is lower than 0.90V. The condition must be held until  $V_{CCPINT}$  reaches 0.40V to ensure PS eFUSE integrity.

For  $V_{CCO\_MIO0}$  and  $V_{CCO\_MIO1}$  voltages of 3.3V:

- The voltage difference between  $V_{CCO\_MIO0}/V_{CCO\_MIO1}$  and  $V_{CCPAUX}$  must not exceed 2.625V for longer than  $T_{VCCO2VCCAUX}$  for each power-on/off cycle to maintain device reliability levels.
- The  $T_{VCCO2VCCAUX}$  time can be allocated in any percentage between the power-on and power-off ramps.

### PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is  $V_{CCINT}$ ,  $V_{CCBRAM}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$  to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If  $V_{CCINT}$  and  $V_{CCBRAM}$  have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If  $V_{CCAUX}$  and  $V_{CCO}$  have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For  $V_{CCO}$  voltages of 3.3V in HR I/O banks and configuration bank 0:

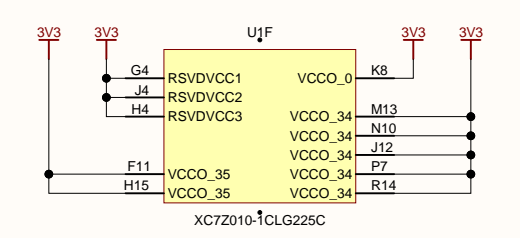
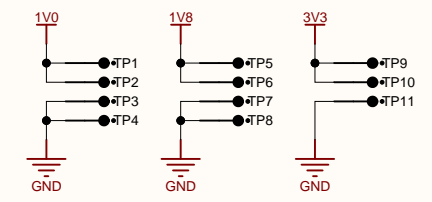
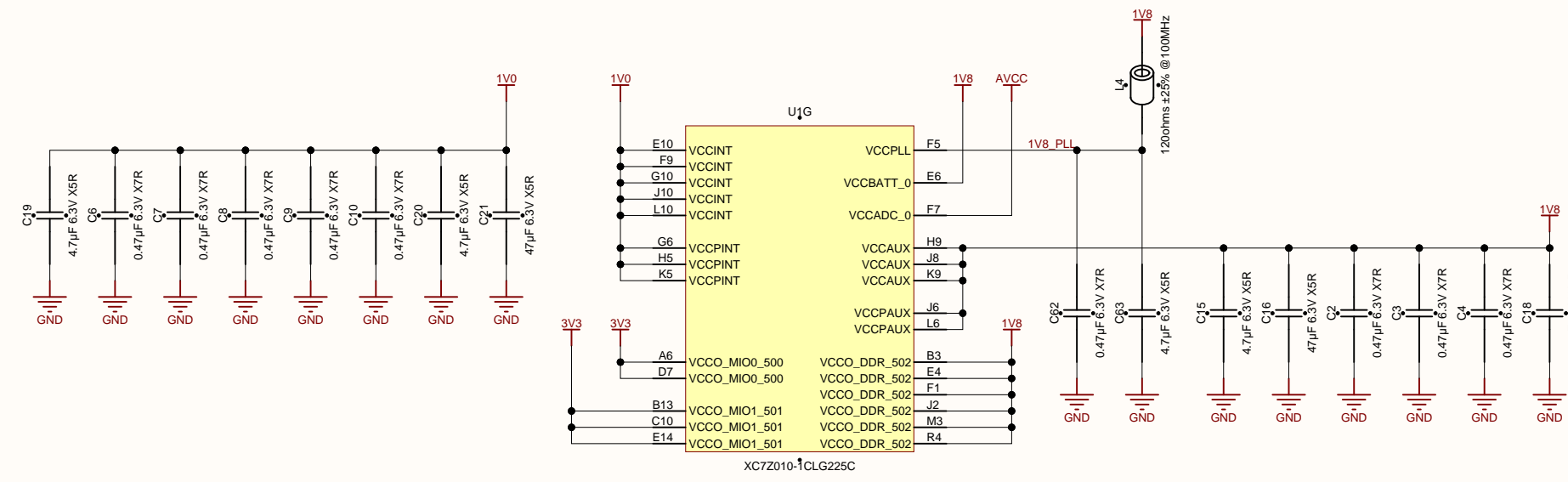
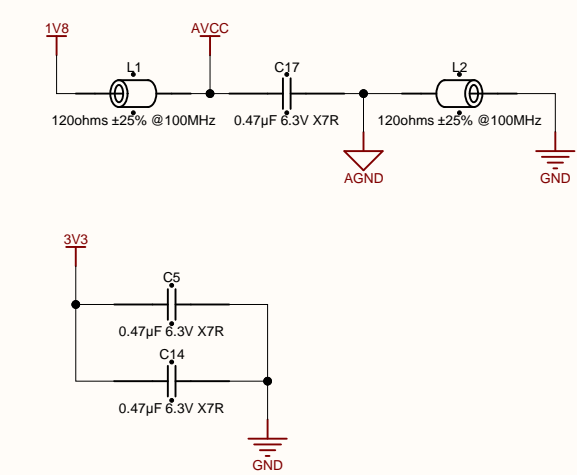
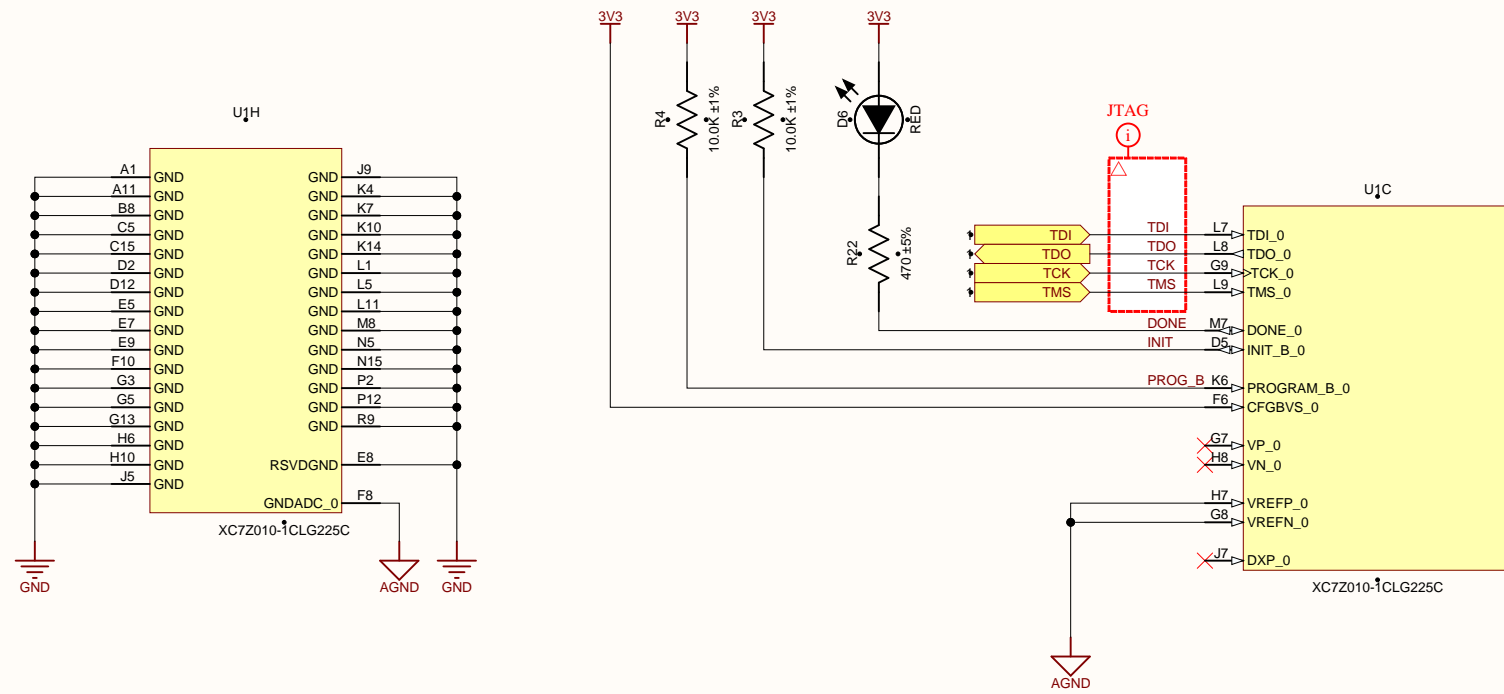
- The voltage difference between  $V_{CCO}$  and  $V_{CCAUX}$  must not exceed 2.625V for longer than  $T_{VCCO2VCCAUX}$  for each power-on/off cycle to maintain device reliability levels.
- The  $T_{VCCO2VCCAUX}$  time can be allocated in any percentage between the power-on and power-off ramps.

# PS/PL Sequencing

PS			PL		
Order	Name	Supply	Order	Name	Supply
1	Vccpint	1V0	1	Vccint	1V0
2	Vccpaux	1V8	2	Vccaux	1V8
2	Vccpll	1V8			
3	Vccmio0	3V3	3	Vcco	3V3
3	Vccmio1	3V3			
3	Vcco_dds	1V8			

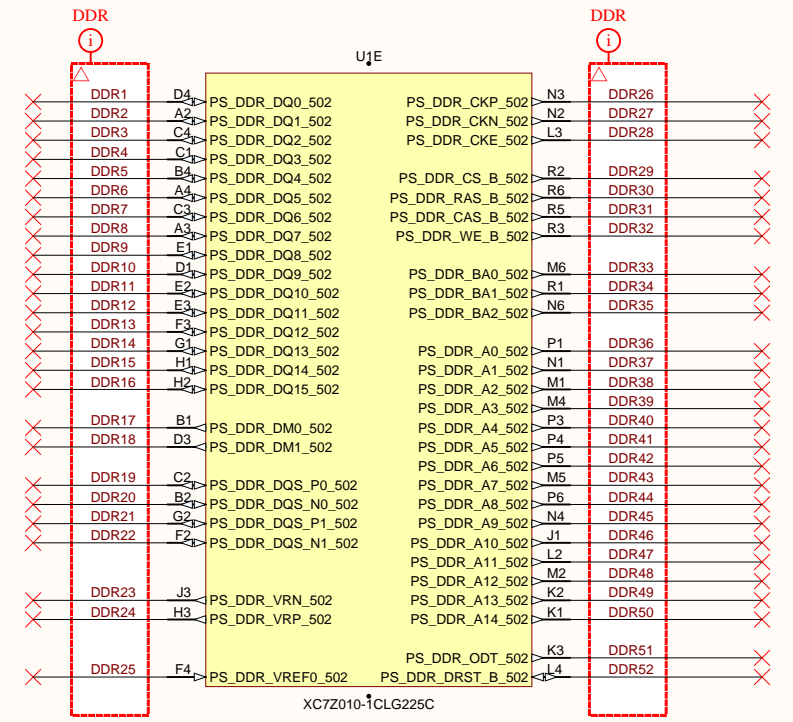
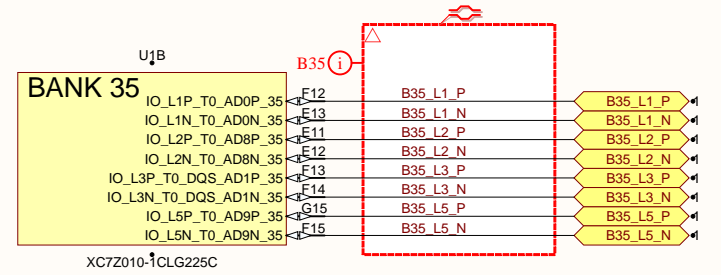
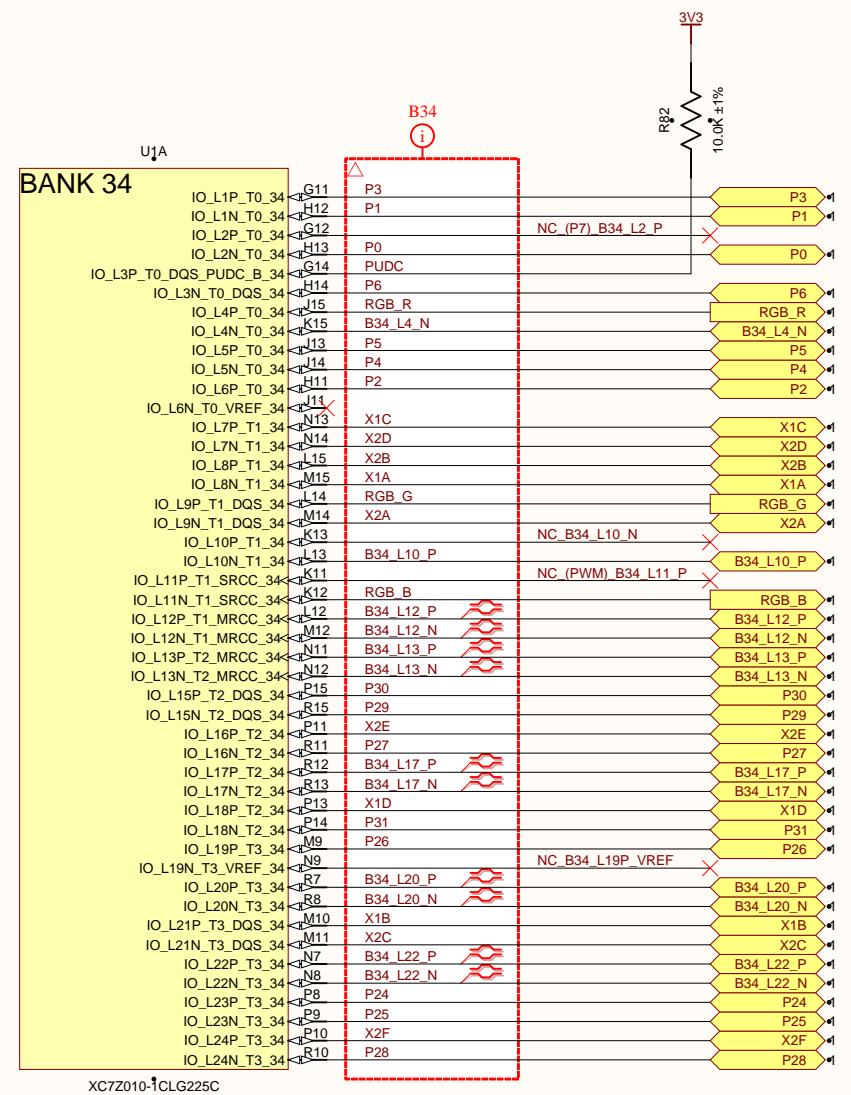
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				PROJECT <b>TDK Zynq 7K Reference</b>		CLIENT PCBA TBD Rev 1	
Title: <b>Power</b>				Morewood Design Labs, Inc. 5001 Baum Blvd. Suite 675 Pittsburgh, PA 15213 412-687-1110		MDL PCB: 20-0001 Fabrication Date:	
Size: B	Number: TBD	Rev 1	Stage FF	Date: 1/10/2020		Sheet 2 of 5	
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<b>PROJECT</b> <b>TDK Zynq 7K Reference</b>				<b>CLIENT PCB A</b> TBD Rev 1	<b>MDL PCB:</b> 20-0001 <b>Fabrication Date:</b>
<b>Title:</b> FPGA Power		Morewood Design Labs, Inc. 5001 Baum Blvd. Suite 675 Pittsburgh, PA 15213 412-687-1110			
<b>Size:</b> B	<b>Number:</b> TBD	<b>Rev:</b> 1	<b>Stage:</b> FF		
<b>Date:</b> 1/10/2020		<b>Sheet:</b> 3 of 5			
<b>File:</b> Zynq 7K Reference FPGA_Power.SchDoc					



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<b>PROJECT</b> <b>TDK Zynq 7K Reference</b>				<b>CLIENT PCBA</b> TBD Rev 1	<b>MDL PCB:</b> 20-0001 <b>Fabrication Date:</b>
<b>Title:</b> B34/B35/DDR					Morewood Design Labs, Inc. 5001 Baum Blvd. Suite 675 Pittsburgh, PA 15213 412-687-1110
<b>Size:</b> B	<b>Number:</b> TBD	<b>Rev:</b> 1	<b>Stage:</b> FF	<b>File:</b> Zynq 7K Reference FPGA_B34_B35_DDR.SchDoc	

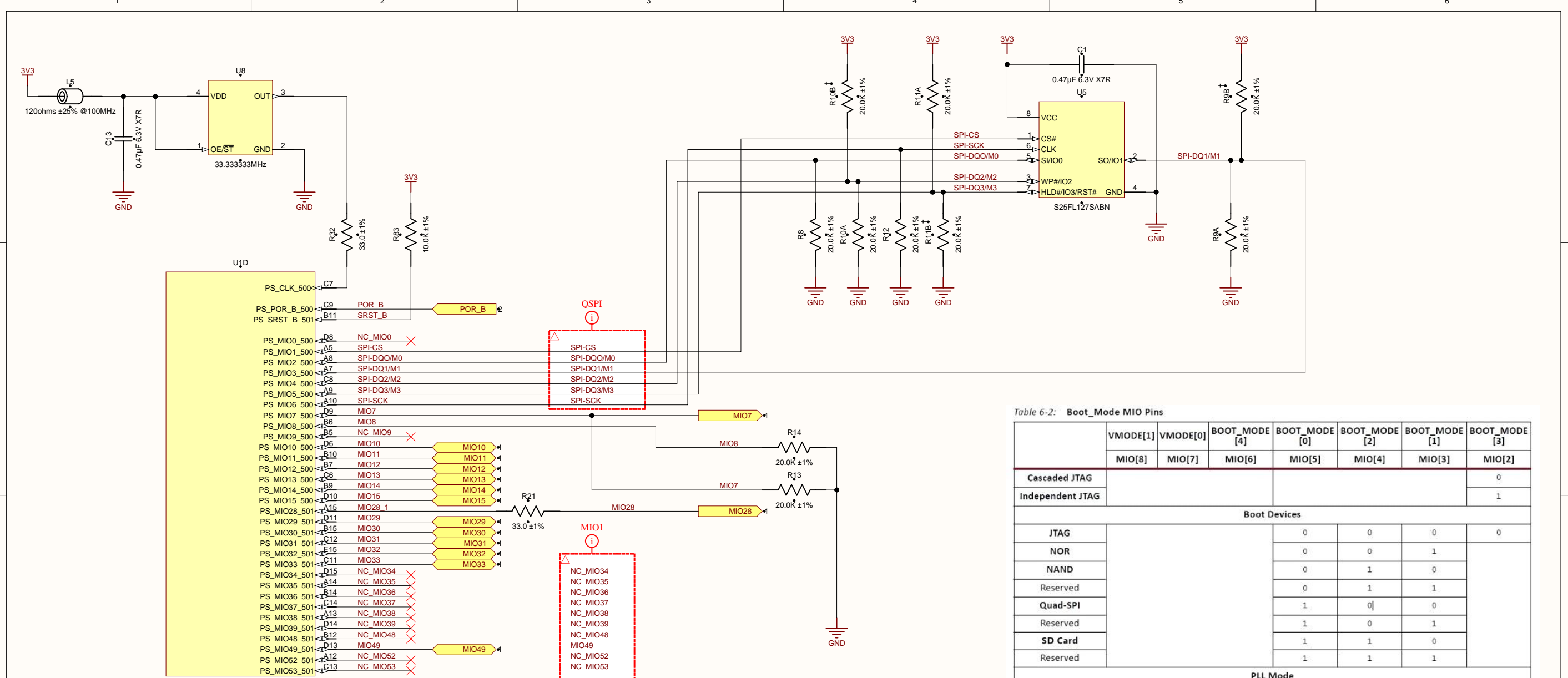


Table 6-2: Boot\_Mode MIO Pins

	VMODE[1]	VMODE[0]	BOOT_MODE [4]	BOOT_MODE [0]	BOOT_MODE [2]	BOOT_MODE [1]	BOOT_MODE [3]
	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
<b>Cascaded JTAG</b>							0
<b>Independent JTAG</b>							1
<b>Boot Devices</b>							
<b>JTAG</b>			0	0	0	0	
<b>NOR</b>			0	0	1		
<b>NAND</b>			0	1	0		
<b>Reserved</b>			0	1	1		
<b>Quad-SPI</b>			1	0	0		
<b>Reserved</b>			1	0	1		
<b>SD Card</b>			1	1	0		
<b>Reserved</b>			1	1	1		
<b>PLL Mode</b>							
<b>PLL Used</b>			0				
<b>PLL Bypassed</b>			1				
<b>MIO Bank 0 Voltage</b>							
<b>2.5 V, 3.3 V</b>			0				
<b>1.8 V</b>			1				
<b>MIO Bank 1 Voltage</b>							
<b>2.5 V, 3.3 V</b>			0				
<b>1.8 V</b>			1				

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		<b>PROJECT</b> <b>TDK Zynq 7K Reference</b>	<b>CLIENT PCB A</b> TBD Rev 1
<b>Title:</b> FPGA MIO		Morewood Design Labs, Inc. 5001 Baum Blvd. Suite 675 Pittsburgh, PA 15213 412-687-1110	
<b>Size:</b> B	<b>Number:</b> TBD	<b>Rev:</b> 1	<b>Stage:</b> FF
<b>Date:</b> 1/2/2020	<b>Sheet:</b> 5	<b>of:</b> 5	<b>MDL PCB:</b> 20-0001 <b>Fabrication Date:</b>
<b>File:</b> Zynq 7K Reference FPGA_MIO.SchDoc			