

REGISTER MAP

| Register | Name | Description | Default Value |
|----------|---|--|--|
| 0C | PVin_report[7:0] | PVin=decimal(Reg0x0C[7:0])/16 | |
| 0D | Vout_report[7:0]Vout=decimal(Reg0x0D[7:0])×0.02+0.6, for Vout>1.8, Vout=decimal(Reg0x0D[7:0])×0.01+0.3, otherwise | | |
| OE | Iout=decimal(Reg0x0E[7:0])/32, for all devices in FS160X except FS1606-0600 Iout_report[7:0] Iout=decimal(Reg0x0E[7:0])/32-(9.05- 0.24×decimal(Reg0x1A[7:2])) ×Vout- 0.356×decimal(Reg0x1A[7:2])+13.1, for FS1606-0600 | | |
| OF | Temp_report[7:0] | Temperature=decimal(Reg0x0F[7:0]) | |
| 10 | Reserved[7:0] | | |
| 11 | Reserved[7:0] | | |
| | Reserved[7:1] | | |
| 12 | Vout_high_byte[0] | Set up 9-bit DAC. Atomic write-protected. So both high byte and low byte have to be written in order to have the value take effect. | |
| 13 | Vout_low_byte [7:0] | | |
| | Reserved[7:4] | | |
| | SS_rate[3] | 0: 0.5mV/µs, 1: 1mV/µs | 'b0 |
| 14 | SoftStopEnable[2] | 0: disable; 1: enable | 'b0 |
| | Reserved[1] | | |
| | PGControl[0] | 0: DAC-based, 1: threshold-based | ʻb1 |
| 15 | Reserved[7:3] | | |
| | OCSet[2:0] | Sets the OCP level for 160X family | ʻb000: FS1603, ʻb001: FS1604, ʻb010: FS1606 |
| 16 | Base_address[7:0] | | 'h08 |
| 17 | Reserved[7:2] | | |
| 17 | OV threshold[1:0] | Vout=decimal(Reg0x0D[7:0])×0.02+0.6, for Vout>1.8, Vout=decimal(Reg0x0D[7:0])×0.01+0.3, otherwise Iout=decimal(Reg0x0E[7:0])/32, for all devices in FS160X except FS1606-0600 Iout=decimal(Reg0x0E[7:0])/32-(9.05- 0.24×decimal(Reg0x1A[7:2])) ×Vout- 0.356×decimal(Reg0x1A[7:2])) ×Vout- 0.356×decimal(Reg0x1A[7:2]))+13.1, for FS1606-0600 Temperature=decimal(Reg0x0F[7:0]) Set up 9-bit DAC. Atomic write-protected. So both high byte and low byte have to be written in order to have the value take effect. 0: 0.5mV/µs, 1: 1mV/µs ′b0 0: 0.5mV/µs, 1: 1mV/µs ′b1 0: 0.5mV/µs, 1: 1mV/µs ′b1 0: 0.5MC-based, 1: threshold-based ′b1 0: 0.5 1: 110, 2: 115, 3: 120 ′b11 0: 105, 1: 110, 2: 115, 3: 120 ′b11 0: 80, 1: 85, 2: 90, 3: 95 ′b10 | 'b11 |
| 18 | Reserved[7:2] | | |
| | PG_threshold[1:0] | 0: 80, 1: 85, 2: 90, 3: 95 | 'b10 |
| 10 | Current_report_offset[7:2] | | |
| 19 | OT_threshold[1:0] | Sets the OTP Threshold, 0: 75, 1: 85, 2: 125, 3: 145 | ʻb11 |
| | Reserved [7:2] | | |
| 1A | Bus_voltage_sel[1] | 0: 1.8–2.5V, 1: 3.3–5V | 'b0 |
| | OV_response[0] | 0:latched, 1:unlatched | 'b0 |
| 1B | Reserved[7:0] | | |

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| Register | Name Description | | Default Value |
|----------|--------------------------|--|---------------|
| | Reserved[7] | | |
| | Unused[6] | | |
| | Unused[5] | | |
| 1C | Reserved[4] | | |
| | Soft_Disable[3] | 0: Soft Enable 1: Soft disable | 'b0 |
| | Unused[2:0] | | |
| | Reserved[7:3] | | |
| 10 | Reserved[2] | | |
| 1D | OTP_clock_on[1] | 1: enable OTP burn (turn on OTP clock) | 'b1 |
| | Vout_max_high[0] | | ʻb1 |
| 1E | Vout_max_low[7:0] | | ʻhC8 |
| | Unused[7:6] | | |
| 20 | User_pointer [5:3] | Read the index of last user bank burned | |
| | Trim_pointer [2:0] | Read the index of last trim bank burned | |
| | Status_pgood[7] | Not sticky, reflects real-time PG status | |
| | Status_ovp[6] | | |
| | Status_ocp[5] | | |
| 21 | Status_otp[4] | | |
| 21 | Status_enable[3] | Not sticky, reflects real-time Enable status | |
| | Status_ncl[2] | | |
| | Clear_status_indicate[1] | | |
| | Status_otp_burn[0] | | |
| 22 | Fb_report[7:0] READ_ONLY | | |
| 23 | Adc_out_vout_lower[7:0] | READ_ONLY | |
| 24 | Adc_out_vout_upper[7:0] | READ_ONLY | |
| 25 | Adc_out_iout_lower[7:0] | READ_ONLY | |
| 26 | Adc_out_iout_upper[7:0] | READ_ONLY | |
| 27 | Adc_out_pvin_lower[7:0] | READ_ONLY | |
| 28 | Adc_out_pvin_upper[7:0] | READ_ONLY | |
| 29 | Adc_out_temp_lower[7:0] | READ_ONLY | |
| 2A | Adc_out_temp_upper[7:0] | READ_ONLY | |
| 2B | OTP_burn[7:0] | OTP to be burned when this register is 0x15 AND OTP_clock_on[0]=1 | |

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Notes:

For soft stop, set Reg 0x1C bit [3] to 0 and toggle Reg 0x14 bit [2] Modifying reserved bits may lead to erratic operation and/or damage

PROGRAMMING INSTRUCTIONS:

- 1) Once all registers are written to desired values, save all the values from Reg 0x12 to reg 0x2B into a configuration file as (register, data) pairs
- 2) Read Reg 0x20

| Reg 0x20 | Number of writes left to OTP |
|----------|------------------------------|
| 0x00 | 4 |
| 0x09 | 3 |
| 0x12 | 2 |
| 0x1B | 1 |
| 0x24 | 0 |

- 3) Apply 7.5V+/-0.25V to Vin pin
- 4) If number of writes left > 0, write 0x15 to Reg 0x2B and then read reg 0x21. If bit [0] is 1, the write to OTP succeeded. If this bit is 0, the write failed.
- 5) If successful, cycle Vin.
- 6) Verify step:

Read registers from 0x12 to 0x1E, compare with the values in configuration file, and verify that they match

- 7) If steps 4 or 6 fail, retry steps 1 to 5.
- 8) If steps 4 or 6 fail again, discard part and debug.

CLOSED LOOP VOUT TRIM:

Scale=1 for FS1606, Vout \leq 1.8V. Scale=2 for FS1606 >1.8 V, and for FS1603, FS1604.

- 1) Vout_target_code_ideal=(Vout_target-0.4*scale)/(0.005*scale)
- 2) Measure Vout
- 3) Vout_err=Vout_target-Vout
- 4) Vout_err_code=Vout_err/(0.005*scale)
- 5) Vout_target_code_adj=Vout_target_code_ideal+Vout_err_code
- 6) Measure Vout, and adjust code until Vout=Vout_target+/-0.0025*scale

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Document revision history

| Revision | Date | Description | Author |
|----------|------------|-----------------------------|-------------------------|
| 0.1 | 11-08-2023 | First draft | Ahmadreza Amirahmadi |
| 0.2 | 03-11-2023 | Modified after final v&v | Ahmadreza Amirahmadi |
| 0.3 | 07-03-2024 | Added Default Values Column | Apoorv Yadav |
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