REGISTER MAP

Register contents

Register	Name	Description
20	i2c_base[6:0]	
21	pmbus_base[6:0]	
22	operation[7:0]	
23	on_off_config[7:0]	
24	write_protect[7:0]	
25	mask_byte_vout[7:0]	
26	mask_byte_iout[7:0]	
27	mask_byte_input[7:0]	
28	mask_byte_temp[7:0]	
29	mask_byte_cml[7:0]	
2A	smb_alert_mask[7:0]	
2B	vout_mode[7:0]	
2C	vout_command_lower[7:0]	
2D	vout_command_upper[7:0]	
2E	vout_max_lower[7:0]	
2F	vout_max_upper[7:0]	
30	vout_margin_high_lower[7:0]	
31	vout_margin_high_upper[7:0]	
32	vout_margin_low_lower[7:0]	
33	vout_margin_low_upper[7:0]	
34	vout_transition_rate_lower[7:0]	
35	vout_transition_rate_upper[7:0]	
36	vout_scale_loop_lower[7:0]	
37	vout_scale_loop_upper[7:0]	
38	vin_on_lower[7:0]	
39	vin_on_upper[7:0]	
3A	vin_off_lower[7:0]	
3B	vin_off_upper[7:0]	
3C	iout_cal_offset_lower[7:0]	
3D	iout_cal_offset_upper[7:0]	

Register	Name	Description
3E	vout_ov_fault_limit_lower[7:0]	OV_threshold = 5% for limit ≤ 10E OV_threshold = 10% for limit ≤ 11A OV_threshold = 15% for limit ≤ 126 OV_threshold = 20% for limit > 126 or for limit <100
3F	vout_ov_fault_limit_upper[7:0]	
40	vout_ov_fault_response[7:0]	
41	vout_ov_warn_limit_lower[7:0]	
42	vout_ov_warn_limit_upper[7:0]	
43	vout_uv_warn_limit_lower[7:0]	
44	vout_uv_warn_limit_upper[7:0]	
45	vout_uv_fault_limit_lower[7:0]	
46	vout_uv_fault_limit_upper[7:0]	
47	vout_uv_fault_response[7:0]	
48	iout_oc_fault_limit_lower[7:0]	
49	iout_oc_fault_limit_upper[7:0]	
4A	iout_oc_fault_response[7:0]	
4B	Reserved[7:0]	
4C	Reserved[7:0]	
4D	ot_fault_limit_lower[7:0]	
4E	ot_fault_limit_upper[7:0]	
4F	ot_fault_response[7:0]	
50	ot_warn_limit_lower[7:0]	
51	ot_warn_limit_upper[7:0]	
52	vin_ov_fault_limit_lower[7:0]	
53	vin_ov_fault_limit_upper[7:0]	
54	vin_ov_fault_response[7:0]	
55	vin_uv_warn_limit_lower[7:0]	
56	vin_uv_warn_limit_upper[7:0]	
57	power_good_on_lower[7:0]	
58	power_good_on_upper[7:0]	
59	unused[7:0]	
5A	unused[7:0]	
5B	ton_delay_lower[7:0]	
5C	ton_delay_upper[7:0]	

Register	Name	Description
5D	ton_rise_lower[7:0]	
5E	ton_rise_upper[7:0]	
5F	ton_max_fault_limit_lower[7:0]	
60	ton_max_fault_limit_upper[7:0]	
61	ton_max_fault_response[7:0]	
62	toff_delay_lower[7:0]	
63	toff_delay_upper[7:0]	
64	toff_fall_lower[7:0]	
65	toff_fall_upper[7:0]	
66	mfr_id_count[7:0]	
67	mfr_id_1[7:0]	K
68	mfr_id_2[7:0]	D
69	mfr_id_3[7:0]	T
6A	mfr_model_count[7:0]	
6B	mfr_model[7:0]	
6C	mfr_revision_count[7:0]	
6D	mfr_revision[7:0]	
6E	capability[7:0]	
78	unused[7:0]	
79	unused[7:6]	
	reserved[5]	
	reserved[4]	
	reserved[3]	
	unused[2:0]	
7A	digital_faults_blank_cycles[7:5]	
	disable_pll[4]	
	pg_mode[3]	0: based on PGood command, 1: based on DAC
	bus_voltage[2]	0: 1.8V to 2.5V, 1: 3.3V to 5V
	bypass_pmbus_dac[1]	If bypass_pmbus_dac is set to 1, use direct_dac_upper and direct_dac_lower instead of bus_voltage.
	direct_dac_upper[0]	
7B	direct_dac_lower[7:0]	

Register	Name	Description
7C	unused[7:4]	
	bypass_adc_filter_1[3]	0: do not bypass; 1: bypass
	Reserved[2:0]	
7D	unused[7:4]	
	bypass_adc_filter_2[3]	0: do not bypass; 1: bypass
	Reserved[2:0]	
7E	unused[7:0]	
88	reserved[7:0]	
89	unused[7:4]	
	unused[3:2]	
	user_otp_on[1]	
	trim_otp_on[0]	
8A	reserved[3:0]	
8B	reserved[7:0]	
8C	reserved[7]	
	unused[6]	
	unused[5:3]	
	reserved[2]	
	reserved[1]	
	clear_status[0]	
8D	unused[7:5]	
	reserved[4]	
	reserved[3]	
	reserved[2:0]	
90	unused[7:1]	
	dac_code_upper[0]	Actual DAC code in 5mV resolution
91	dac_code_lower[7:0]	
92	unused[7:6]	
	user_pointer [5:2]	1 to A
	trim_pointer [1:0]	1 to 5

Register	Name	Description
93	status_pgood[7]	
	status_ovp[6]	
	status_ocp[5]	
	status_otp[4]	
	status_enable[3]	
	status_trim_burn[2]	
	status_user_burn[1]	
	clear_status_indicate[0]	
94	ic_rev_byte_count[7:0]	
95	ic_rev[7:0]	
96	ic_dev_id_count[7:0]	
97	ic_dev_id[7:0]	
98	Reserved]7:0]	
99	Reserved]7:0]	
9A	pvin_report_lower[7:0]	$\frac{1}{16}$ V resolution
9B	pvin_report_higher[7:0]	
9C	Reserved]7:0]	
9D	Reserved]7:0]	
9E	Reserved]7:0]	
9F	Reserved]7:0]	
A0	vout_report_lower[7:0]	$\frac{1}{256}$ V resolution
A1	vout_report_higher[7:0]	$\frac{1}{256}$ V resolution
A2	temp_report_lower[7:0]	1°C resolution, two's complement for negative temperatures
A3	temp_report_higher[7:0]	
A4	vcc_report_lower[7:0]	$\frac{1}{32}$ V resolution
A5	vcc_report_higher[7:0]	
A6	addr_report_lower[7:0]	
A7	addr_report_higher[7:0]	

Programming instructions

1) Once all registers are written to desired values, read all the values into a configuration file as (register, data) pairs.

2) Read Reg 0x92 to check number of available trim banks.

Reg 0x92[3:0]	Remaining writes (trim section)
0001	4
0010	3
0011	2
0100	1
0101	0

3) Read Reg 0x92 to check number of available user banks.

Reg 0x92[7:4]	Remaining writes (user section)
0001	9
0010	8
0011	7
0100	6
0101	5
0110	4
0111	3
1000	2
1001	1
1010	0

4) Apply 7.5V ± 0.25V to V_{IN} pin.

5) If number of trim writes left > 0, write 0x01 to reg 0x89.

6) Read reg 0x93. If bit [2] is 1, the write to OTP succeeded. If this bit is 0, the write failed.

7) If successful, cycle V_{IN}.

8) Read all registers, compare with the values in the configuration file, and verify that they match.

9) If step 6, 8 or 10 fails, retry steps 1 to 5.

10) If step 8 or 10 fails again, discard the part and debug.

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